A Study on the Performance of Delta Modulation Systems

by

Hazm Anwar Elahi

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In

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THE UNIVERSITY OF PETROLEUM AND MINERALS

GRADUATE SCHOOL

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A THESIS
SUBMITTED TO THE GRADUATE SCHOOL
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE
DEGREE OF
MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

BY
HAZM ANWAR ELAHI
DHAHRAN - SAUDI ARABIA
JUNE 1980

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COLLEGE OF GRADUATE STUDIES

This thesis, written by Hazm Anwar Elahi under the direction of his Thesis Committee, and approved by all its members, has been presented to and accepted by the Dean of College of Graduate Studies in partial fulfillment of the requirements for the degree of M.S. in Electrical Engineering.

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THIS THESIS IS DEDICATED TO MY PARENTS AND MY WIFE

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Abstract

The basic principles of linear and companded delta modulation systems are presented. Also described are continuously variable slope delta modulators, built as integrated circuits by Motorola and Harris Semiconductors. Design techniques for linear systems and for the continuously variable slope delta modulator systems are included as well.

The test results for the three systems (discrete element linear, Motorola integrated circuits, and Harris integrated circuit) are presented. Three different operating conditions are considered; i.e. idling, normal operating, and slope overloading. Methods to theoretically predict the transfer function characteristics for each system are also described.

Possibilities of changing the performance of the systems are also considered in terms of various control parameters. These parameters are the sampling rate, the loop gain, the syllabic filter time constant, and the shift register length.

CHAPTER - 1

INTRODUCTION AND BACKGROUND

1-1. The Need for Digital Communication Techniques

As man became capable of sending messages to far distances, communication engineers sought better techniques so that these messages reached distant parties with maximum clarity. Techniques of modulation, as amplitude modulation (AM) or frequency modulation (FM), were initially used to achieve signal transmission over long distances. In both of these modulating procedures the modulated signal has a continuous (analogue) form. This analogue signal, while being transmitted, is subjected to various kinds of distortions due to interferences within the long distances, fading or any other atmospheric conditions, induction noise if land lines are used, and noise amplification at repeating stations along the transmission path.

In communication systems, the influence of interferences in the transmission path can be reduced considerably by coding the information signal first and then transmitting a corresponding pulse pattern of 0 and 1 pulses, or in other words digitizing (quantizing) the analogue signal. H.R. Schindler |1| has stated that A.H. Reeves first proposed the conversion of analogue signals into digital format in 1938. In doing so, he clearly defined the concept of pulse code modulation (PCM) and recognized its advantages. This "digital technique" is now frequently used. Digital techniques depend on detecting the presence or absence of a pulse of fixed amplitude. This results in a much improved immu-

nity to noise interference and other distortions. Many other technical advantages can be claimed for digital systems, there are |1|:

* There is little concern over accumulation of noise and distortion, since the binary or two level signal can be easily regenerated or reshaped with only a small probability of error.

* Time-division multiplexing of digital information frequently leads to economical use of cables. Compared with frequency-division multiplexing, no complex filters are required in the digital case, since all the multiplexing and demultiplexing functions can be accomplished with digital circuitry.

* Switching of digital information can be easily realized with digital building blocks. This leads to fully electronic exchanges (Telephone and Telex). Many problems of present-day exchanges such as analogue crosstalk and mechanical contacts, can thus be avoided.

* Information in digital form can be scrambled easily. This is important whenever privacy or secrecy must be guaranteed, especially in military communications.

* Transmission of information over futuristic carriers, such as laser beams or long-distance waveguides, is best accomplished in digital form.

* The power required to operate the system is low compared to analogue systems.

* Another advantage of the digital system is the economy in the cost of the terminal hardware. Micro-circuit logic elements developed for the computer industry in large quantities and low cost make the use of digital circuitry very inexpensive compared to analogue circuitry of conventional systems.

1-2. Delta Modulation Systems

1-2.1 General definition

Pulse code modulation is a digital technique that is the most well-known method for communication systems |1|. It is widely used as a means of transmission through telecommunication channels. The analogue information is sampled at regular time intervals by an intermediate process known as "Pulse Amplitude Modulation" (PAM) and then these samples are coded into binary words, according to the signal's amplitude.

Delta modulation (DM) was conceived as a simple alternative to pulse code modulation. It was invented in 1946 |2| and is discussed in various papers |1,3,4|. The system consists of an encoder and a decoder commonly called "Codec". The encoder is a closed loop data control system which generates single bit quantized words, representing the sign of the error in a tracking signal rather than the actual input signal value. The transmitted pulses contain information in their arithmetic density, i.e. the average pulse density is proportional

to the slope of the input signal. A simple transmitting system which uses delta modulation technique is shown in Fig. 1-1, whereas its watching waveforms for an input analogue signal x(t) is shown in Fig. 1-2.

Delta modulator is much simpler to implement than PCM, since the PAM and the binary coding process are avoided. It is nearly as effective as PCM and the simpler circuitry of encoding and decoding result in a very low cost. Because of its tolerance to transmission error, it is in some situations preferable to PCM. Table 1-1 gives a short comparison between DM and PCM systems |5|.

Characteristic	Modulation	
	Delta	PCM
Ability to time-share encoder among multiple channels.	Unsuitable	Suitable
Dependence on frequency components of signal being encoded.	Overloads in presence of high-amplitude, high-frequency components.	Essentially
Cost	Lower.	Higher.
Word synchronization requirement.	No.	Yes.
Tolerance to transmission error.	Good.	Poor.
S/N ratio at low transmission bit rates.	Higher.	Lower.
S/N ratio at high transmission bit rates.	Lower.	Higher.
Suitability for encryption.	Better.	Poorer.
Requires accurately synchronized transmitter and receiver for signal channel transmission.	No.	Yes.
Reconstruction and filter requirements.	Simple.	Complex.

Table 1-1 - Comparison of DM and PCM systems.

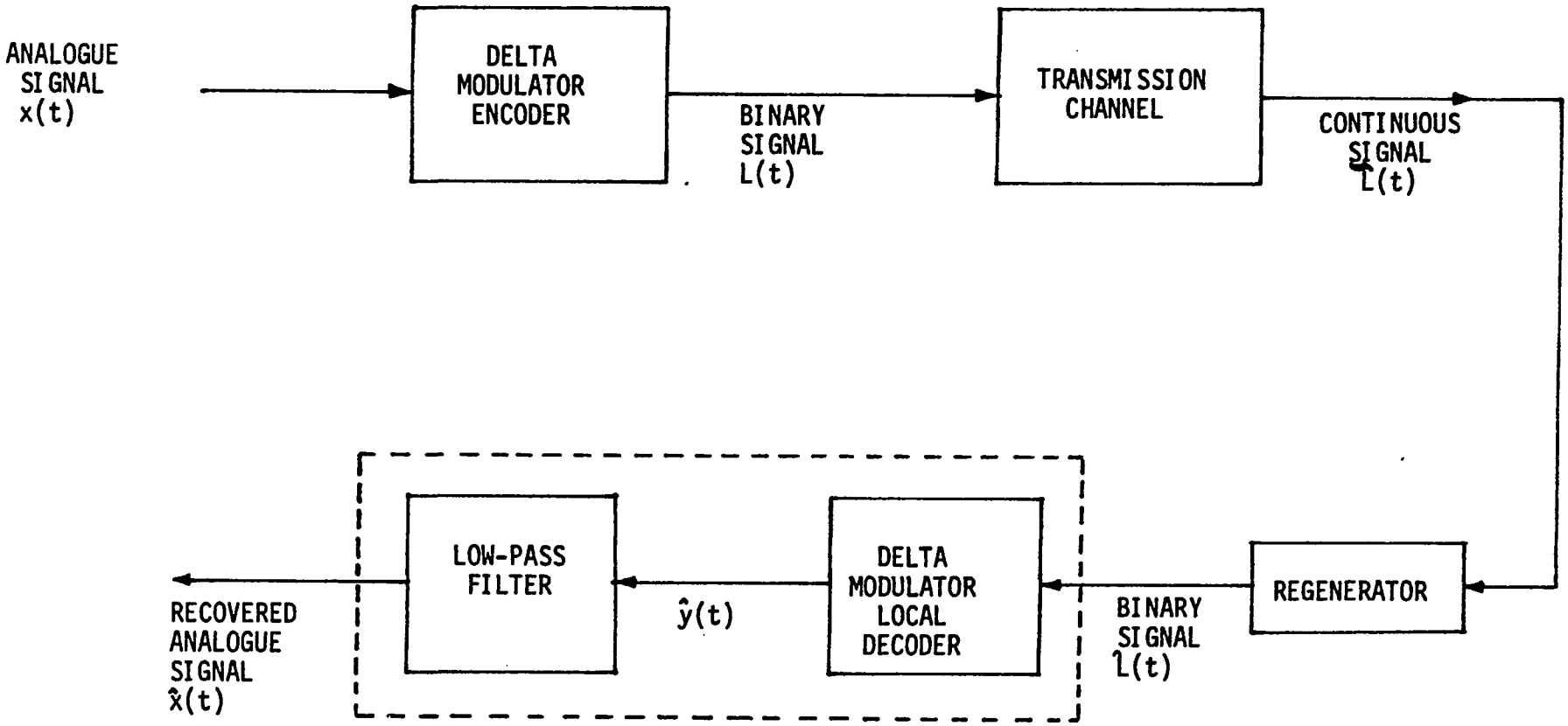


FIG. 1-1 Simple Transmitting System.

A delta modulator produces a single binary signal L(t) from an analogue input signal x(t). The binary signal, degraded by transmission, is reshaped by the regenerator, decoded, and then filtered into a close replica of the original analogue signal.

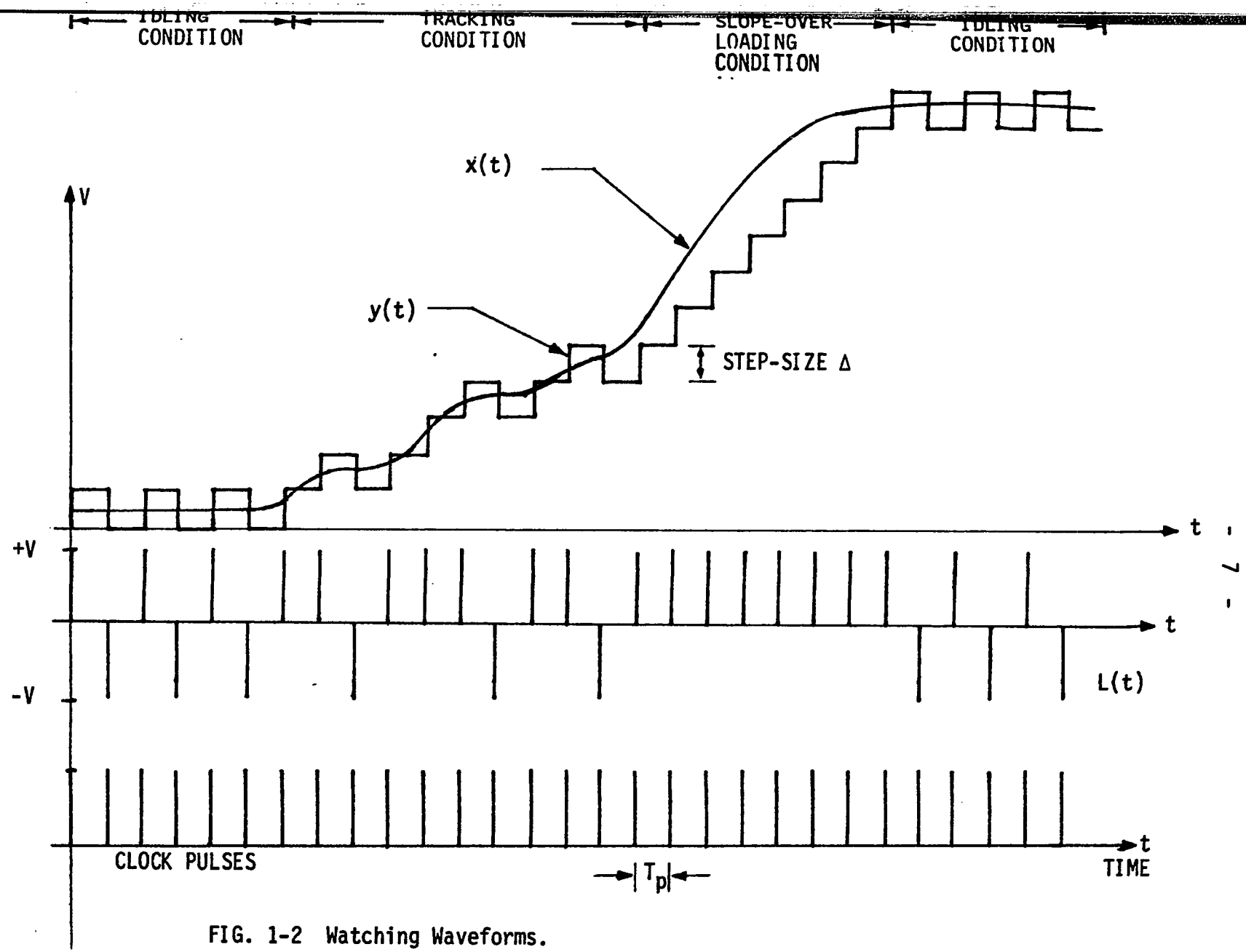


FIG. 1-2 Watching Waveforms.

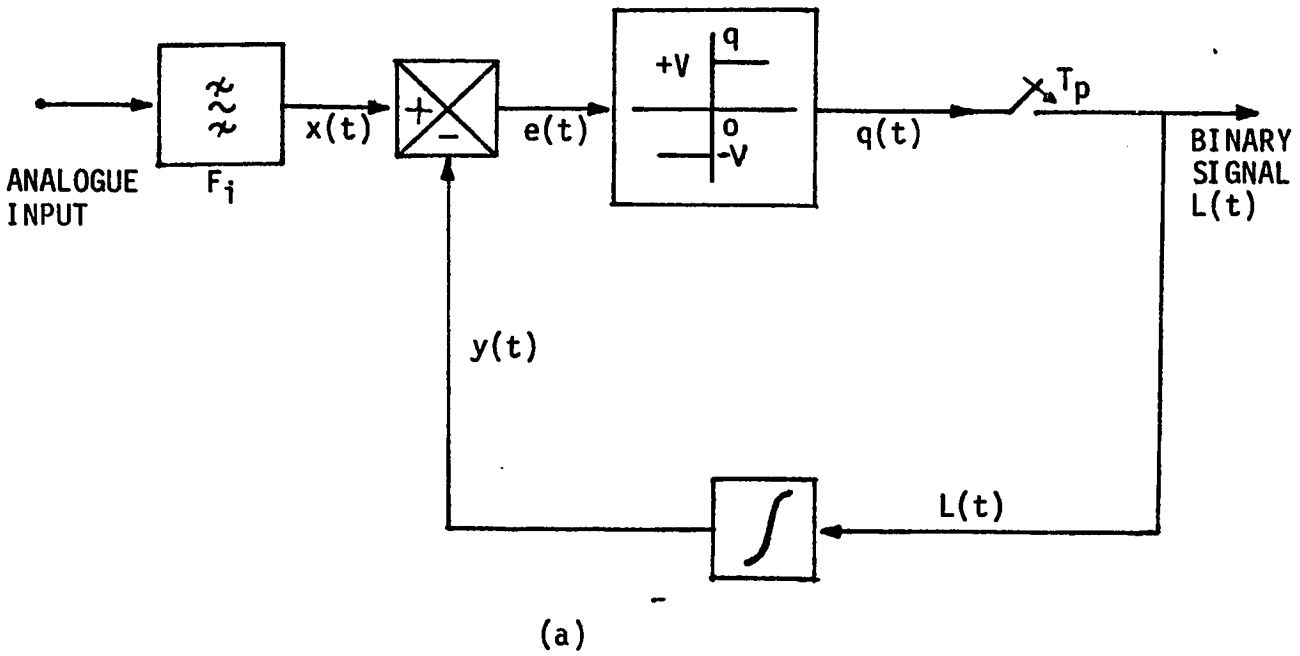
With no input, the tracking signal y(t) is a series of steps corresponding to a binary signal L(t) of equal and opposite levels. In the tracking condition, the feedback signal attempts to track input signal x(t). In slope-overloading condition the y(t) fails to track the input and rises in steps to catch it.

The main impetus for the use of DM has come from the telecommunications industry for binary encoding and decoding of speech and video signals, numerous applications in industrial control, mobile communication, and measurement instrumentation exist as well. These applications include:

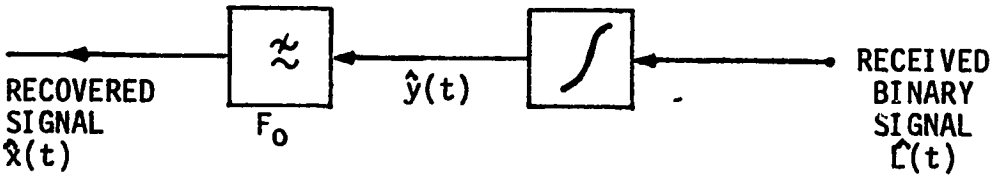
* Digital filters.
* Remote control
* Scrambling of speech signals.
* Encoding transient signals for storage and display.
* Compressing the amplitude range of an analogue signal.
* Delaying an audio signal by different amounts to produce a reverberated sound (echos).
* Encoding signals for acoustic modems.
* Encoding photographic profiles of objects for computer processing.
* Uses in instruments like voltmeters, wattmeters, etc.

1-2.2 The concept of delta modulation system

The encoder of a DM system is a closed loop control system, where instead of the absolute signal being transmitted at each sampling instant, only the change in signal amplitude from sampling instant to sampling instant is transmitted in binary or two level pulses. Fig. 1-3 shows the simplest form of DM system which is known as "Linear Delta Modulation". Actually all delta modulators are non-linear systems, but a system similar to that shown in fig.1-3



(a)



(b)

FIG. 1-3 Linear Delta Modulation System

a) Encoder
b) Decoder

is called linear since the local decoder producing the feedback signal is a linear network. The delta modulator acts as an analogue to digital convertor. A band limited signal x(t), having critical frequencies at f_{c1} and f_{c2} such that $f_{c2} > f_{c1}$, forms the input analogue signal. The waveform L(t), at the output of the delta modulator, consists of pulses of duration T seconds and spaced T_p seconds apart such that $T_p >> T$ The L(t) amplitudes are either $\pm$ V volts. These pulses occur at a clock rate $f_p = \frac{1}{T_p}$, where f_p needs to be considerably greater than the Nyquist rate; i.e. $2f_{c2}$ |4|. The relation between x(t) and L(t) is such that L(t) is a binary transformation on x(t), where the rate of occurance of the binary pulses is directly proportional to the instantaneous slope of x(t). If the slope of the input signal x(t) is positive, then the output waveform L(t) has more positive pulses than negative ones. This situation is reversed when x(t) has a negative slope. At maxima and minima, where the slope is close to zero, there are equal numbers of positive and negative L(t) pulses.

The decoding network in DM system usually consists of a network similar to the local decoding network existing in the feedback loop of the encoder, followed by a band-pass filter F_o. The output filter is necessary to eliminate the high frequency components. For properly designed systems, the recovered signal is a close replica of the input signal and will differ only by a relatively small amount of error.

1-2.3 Principle of operation

Consider the system shown in Fig. 1-3, which generates digital impulses having an area of $\pm$ RCΔ volt-sec. (where RC is the time constant of the integrator used in the feedback loop). The positive impulses represent the "1" state, while the negative impulses represent the "0" state. When these impulses are integrated in the feedback loop, positive and negative steps having a duration of T_p seconds and amplitude of Δ volts will result, such that:

$$\Delta = VT/RC \qquad (1.1)$$

where: V is sufficiently large to appear as an impulse to the integrator,

T is the pulse width of $\bar{L}(t)$ and much less than T_p

The integrated signal y(t) and the input analogue signal x(t) are compared by a differential amplifier to produce an error signal e(t):

$$e(t) = x(t) - y(t) \qquad (1.2)$$

The error signal is quantized to predetermined positive or negative values by a threshold comparator such that:

$$q(t) = V \quad \text{if} \quad e(t) \geq 0 \qquad (1.3)$$
$$= -V \quad \text{if} \quad e(t) < 0$$

Equation 1.2 indicates that the system is sensitive to only the sign and not the magnitude of the error signal. The output of the quantizer is sampled every T_p second to produce the L(t) pulses.

If $e(t) \geq 0$ at a clock instant, a positive pulse L_r will be produced at the output of the encoder. When this pulse is integrated y(t) increases by a positive step. The increase in y(t) will be subtracted from x(t) and a change in the magnitude of the error signal occurs. If the error has not become negative by the next clock instant the output of the encoder will again be a positive pulse. As long as $e(t) \geq 0$ at successive clock instants, a sequence of positive pulses will be produced. Eventually y(t) will become greater than x(t). At a clock instant where $e(t) < 0$, a negative pulse will occur at the output of the encoder, resulting a diminution in the y(t) waveform. Thus, the encoder attempts to minimize the waveform error e(t) by varying the polarity of the pulses at the output of the modulator at clock instants.

Assuming errorless transmission, the $\hat{L}(t)$ signal at the receiver is integrated to give $\hat{y}(t)$. This $\hat{y}(t)$ signal is identical to y(t) in the encoder. As y(t) differ from the input signal x(t), the system will produce an error signal e(t). If the error is small, the signal at the output of the integrator in the decoder is a good reproduction of the original input signal. The step-like nature of $\hat{y}(t)$ is removed by passing it through a filter, whose band-pass frequency is the same as that of the input message i.e. filters F_i

and F_0 may be considered to be identical. Further simplification may be added to the decoder by making the filter F_0 a low-pass rather than a band-pass one. This is because the noise below f_{c1} is generally not troublesome. This simplicity of the decoder in linear DM is one of its attractions particularly because the reconstruction network is merely an integrator with just a resistor and capacitor. A PCM system requires a network which is more complicate than just an integrator to reconstruct the digitally coded waveform.

1-3. Performance Criteria of DM Systems

1-3.1 Overview

An important design consideration is noise generated within a DM system. This noise can be broken into two distinct areas; quantization noise, accompanying a signal, and idle channel (zero input signal) noise. Two major parameters which effect performance are the sampling rate f_p and the step-size Δ. Ideally Δ should be as small as possible and f_p as large as possible. A design criterion is that the product $\Delta.f_p$ should exceed the maximum slope of the input waveform. Practical and economic considerations limit the minimum size of Δ and the maximum rate f_p. These limitations give rise to two types of distortions, slope overload noise and quantization or granular noise.

1.3.2. The idling behaviour

The DM system is in its idling state when the analogue input signal is constant or zero. The idling pattern of the linear DM system is composed of alternating positive and negative pulses; i.e. 1 0 1 0 1 0 . . . etc. |6,7|. The logical one's and zero's refer to positive and negative pulses of the L(t) waveform, respectively. The feedback network generates a feedback signal y(t) which is nearly a rectangular wave having a period of $2T_p$ and an amplitude of $\pm \Delta/2$. The error signal, with a zero input x(t) signal is therefore:

$$e(t) = -y(t) \qquad (1.4)$$

whereas for a constant input signal, it is given by equation 1.2. The result is that the waveform at the output of the quantizer is also a rectangular wave having the same frequency as that of the error signal but with positive and negative amplitudes equal to V.

An encoder whose idling pattern is composed of 1 0 1 0 1 ... is known as a symmetrical encoder i.e. the plus and minus quanta (step) fed to the integrator are exactly equal in magnitude. Due to poor design, two adjacent one's or zero's can be found in some encoders. These encoders are known as assymmetrical encoders. The feature of the symmetrical encoders is that when an analogue signal is applied, the slope required to produce an all one's pattern has the same magnitude and opposite polarity as the slope which will produce an all zero's pattern. The symmetry and assymmetry of a codec is

considered to result from the quantizer characteristics shown in fig. 1.4. Even if the quantizer is symmetric the output of the decoder can still have a waveform comparable to an assymmetric quantizer if the integrators are assymmetric with respect to positive and negative inputs. This may be caused, for example, by different gains, time constants, etc.

The idling pattern and its y(t) waveform for symmetrical and assymmetrical encoders of LDM system, are shown in fig. 1.5. Other types of amplitude modulation would occur for non-linear delta modulators.

In the decoding network, the idle channel pattern is integrated and then rejected by the final filter. This rejection occurs because the fundamental frequency of the binary signal L(t) is $f_p/2$ HZ. Hence, neither this lowest frequency in the signal nor the higher frequency components will be able to pass through the filter, having an upper frequency of f_{c2} which is much less than $f_p/2$. Practical filters do not have infinite attenuation at $f_p/2$. Consequently a non-zero output signal will exist in the idle condition. If the encoding and decoding process are assymmetrical, i.e. the idle channel pattern is somewhat similar to fig. 1-5b, then y(t) can be considered to be the sum of the idle condition waveform and a sawtooth waveform at fundamental frequency f_y given by |4|:

$$f_y = \frac{1}{\lambda} \left[\frac{\Delta-\mu}{\mu} + 1 \right]^{-1} \cdot f_p \qquad (1.5)$$

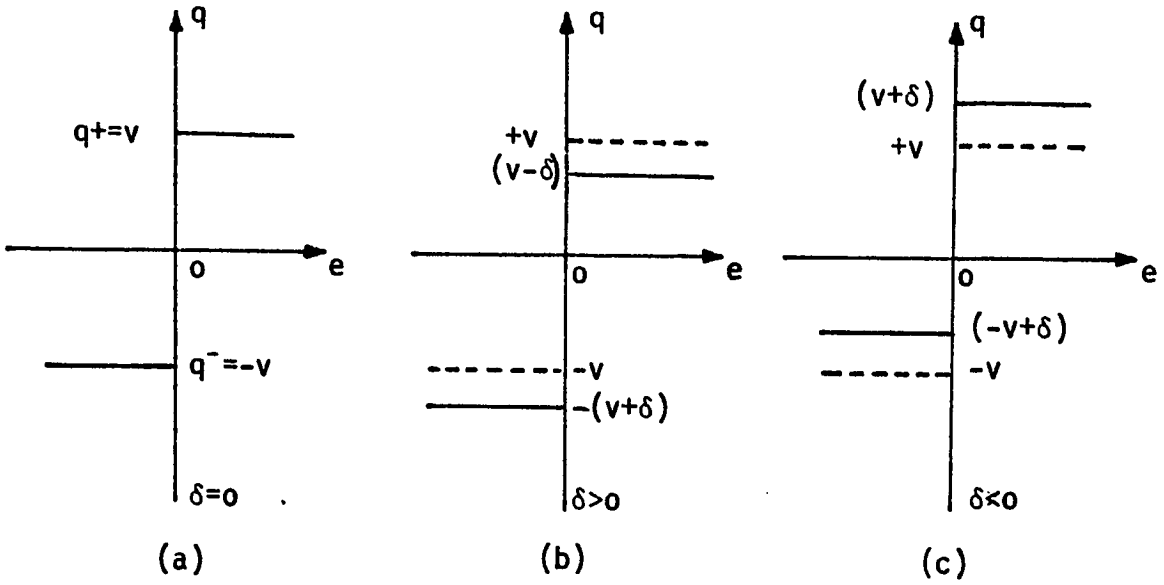


FIG. 1-4 Quantizer Characteristics

a) Symmetrical encoder where $q+=q^-=v$

b) Assymmetrical encoder having assymmetry in the negative direction, i.e. $q+<q^-$.

c) Assymmetrical encoder having assymmetry in the positive direction, i.e. $q+>q^-$

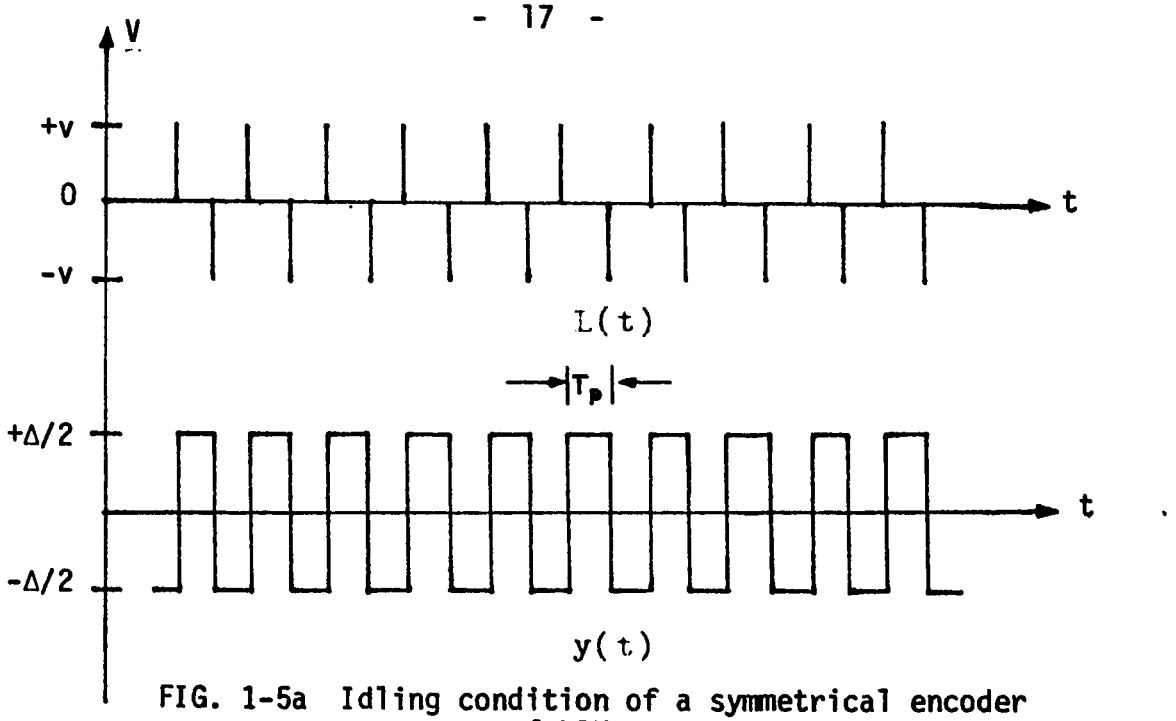


FIG. 1-5a Idling condition of a symmetrical encoder of LDM system

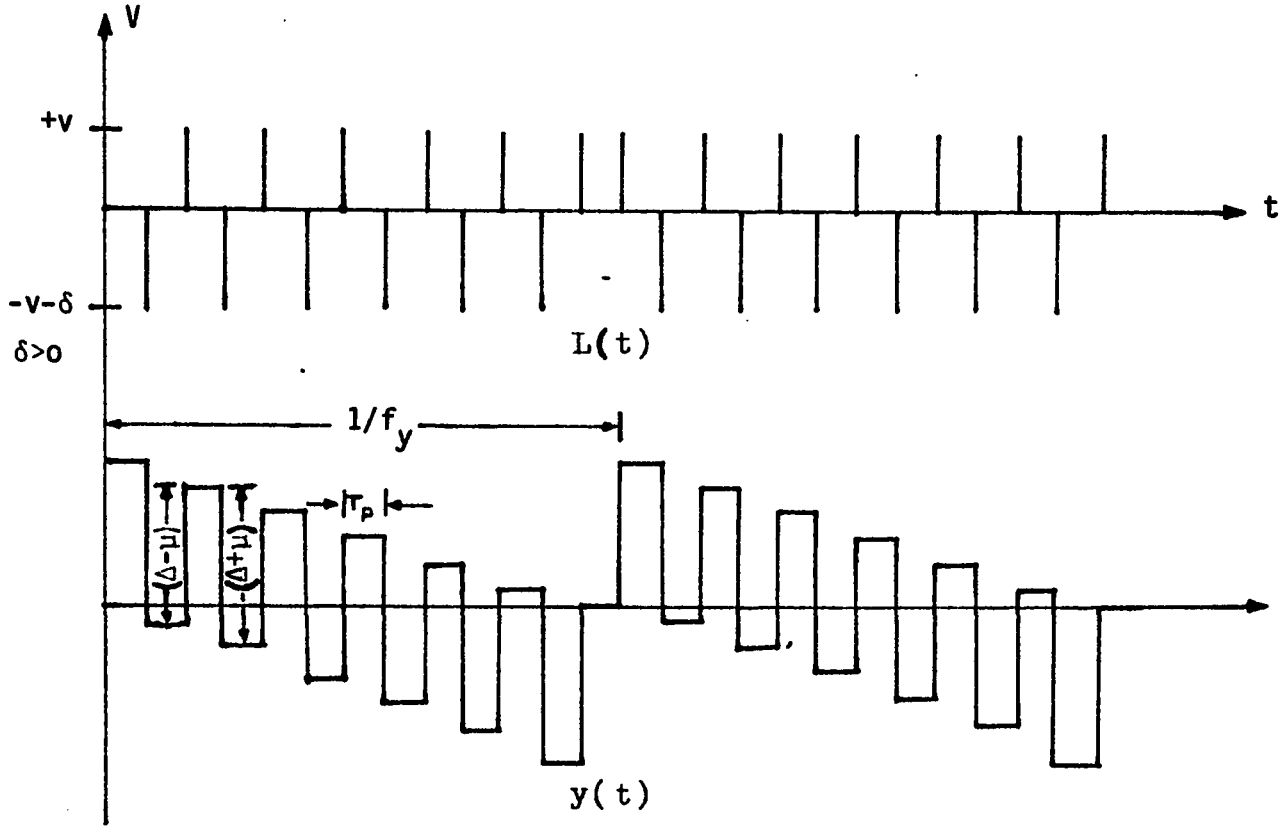


FIG. 1-5b Idling condition pattern of an assymmetrical encoder of a LDM system

Where: λ is the number of positive peaks in the periodic pattern of $y(t)$ and μ is the error of the output of the integrator after one clock period.

Even with filtering this waveform, an unwanted signal component $i(t)$, at frequency equal to that of the sawtooth waveform, will emanate at the decoder output. This $i(t)$ signal is called the idle condition noise. The presence of the idle condition noise degrades the performance of the DM system. By careful design this type of noise can be reduced to zero or at least to negligible proportions.

1-3.3 Slope overloading behaviour

In DM systems the rate of occurance of each binary level is related monotonically to the slope of the analogue input signal. Fig. 1.6 shows the behaviour of the encoder shown in fig. 1-3a, where the input is sinusoidal and the encoder is correctly tracking the input. The pulses composing the binary output waveform are drawn for convenience having negligible width T and the integrator is assumed to have very large discharge time constant so that the response to an impulse is practically a unit step. The encoder attempts to generate an $L(t)$ pattern whose mean value approximates the mean value of the slope of the sinusoidal input over a short period of time. Should the slope of the input signal increase or decrease so fast that the feedback signal cannot track the input signal, a stream of output

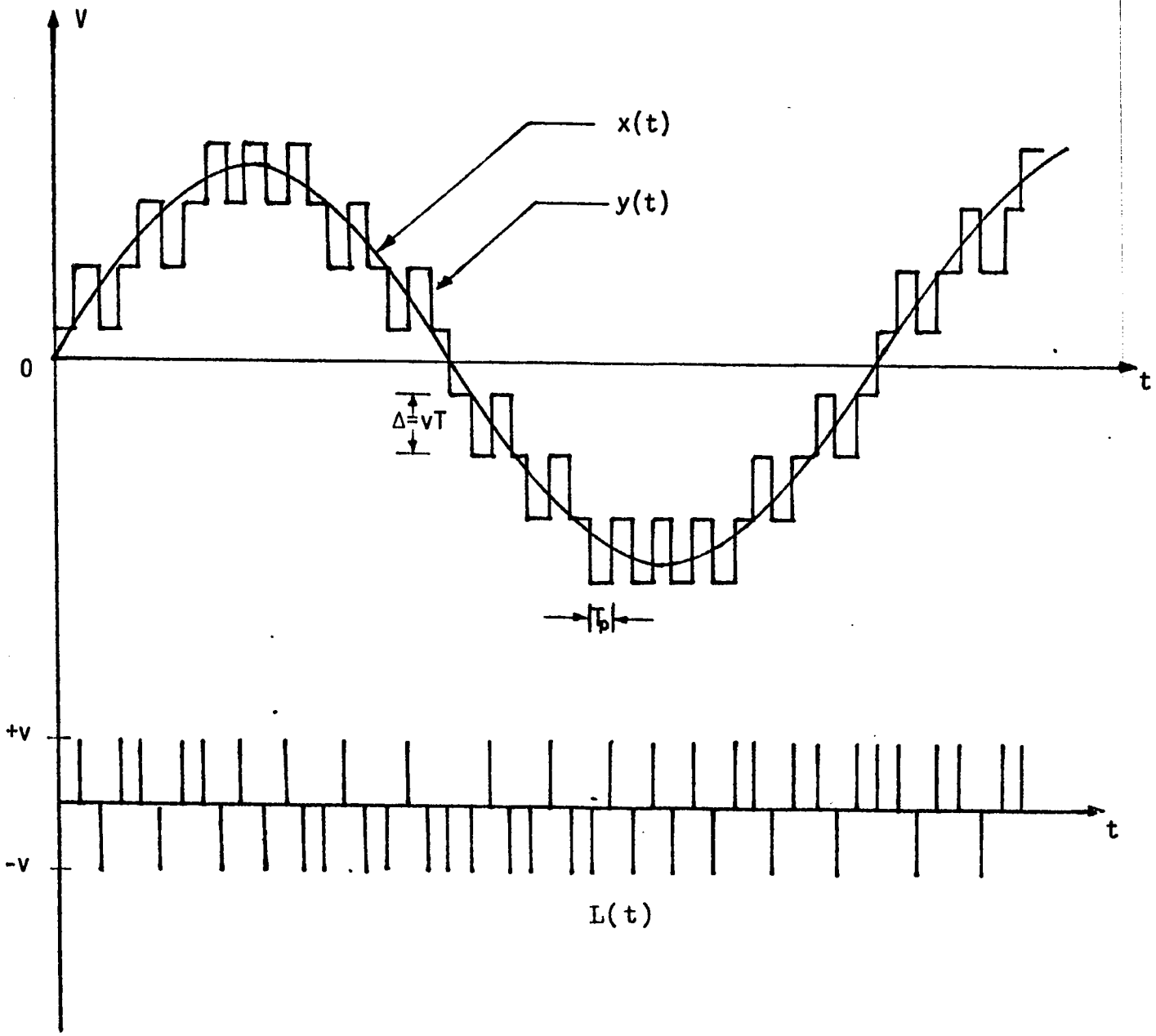


FIG. 1-6 Waveforms when the encoder is tracking a sinusoidal input signal x(t).

bits of identical polarity are generated by the encoder. An encoder generating such pattern is said to be "slope overloaded". Fig. 1-7 illustrates the case when a linear delta modulator is completely overloaded (although fig. 1-7 applies for LDM, similar phenomena occur for non-linear types) by a sinusoidal signal whose instantaneous value is given by:

$$x(t) = E_s \sin w_s t \qquad (1.6)$$

Where: $w_s = 2\pi f_s$ is the angular frequency of the input signal and E_s is its peak value.

In order to avoid slope overload, the slope capability of DM system must be greater than the slope of the input signal. Since the former is given by the product of step-size Δ and sampling rate f_p, then to avoid slope overloading the following condition must be satisfied for all t |8|:

$$\Delta . f_p > |\dot{x}(t)| \qquad (1.7)$$

Where: $|\dot{x}(t)|$ is the magnitude of the derivative with respect to time of the input analogue signal x(t). For the sinusoidal input given by equation 1.6 the above condition can be rewritten as:

$$\Delta . f_p = 2\pi f_s E_s \qquad (1.8)$$

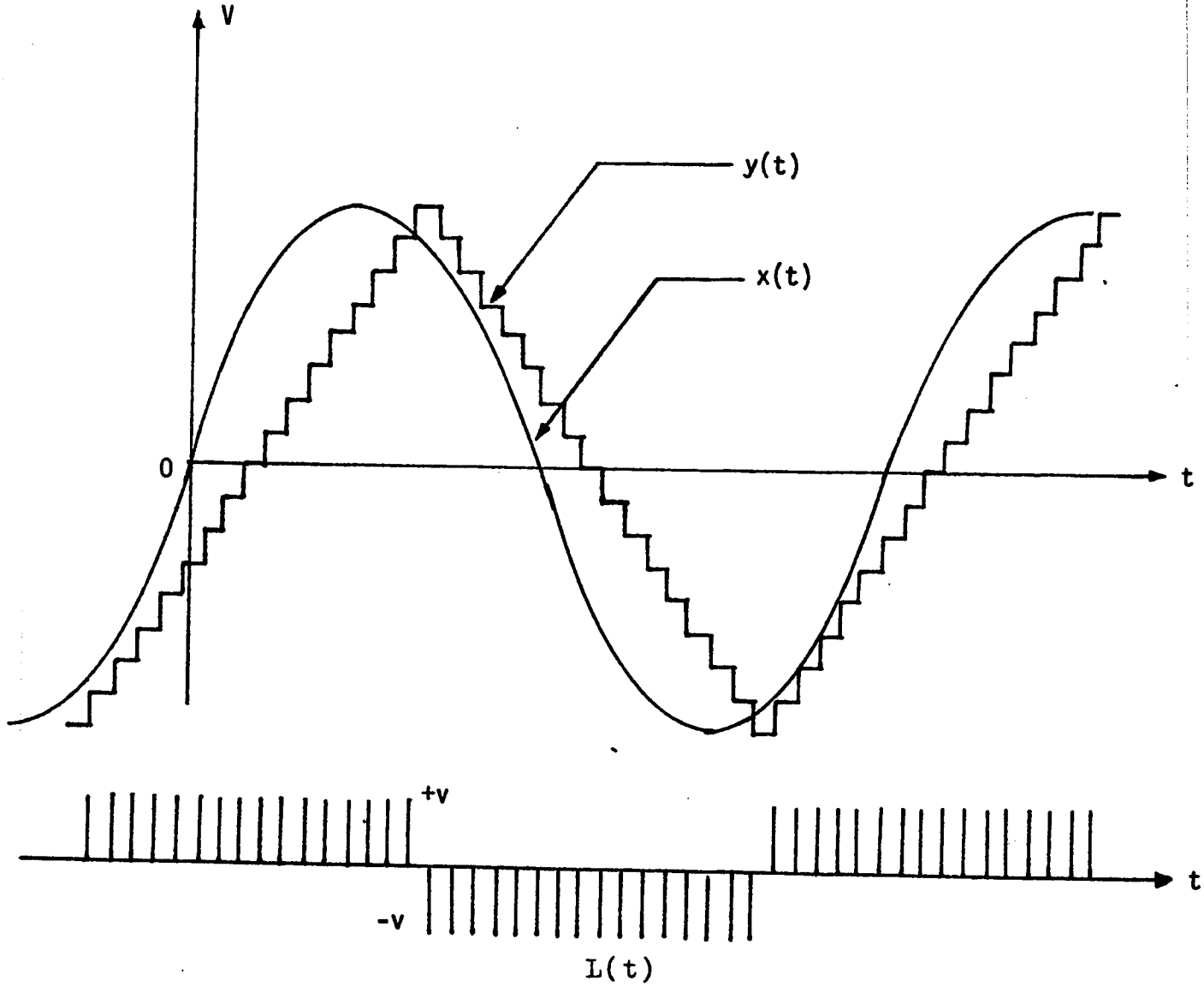


FIG. 1-7 Waveforms when the encoder is substantially slope overloaded by a sinusoidal input signal x(t).

Which shows that slope overloading can be avoided as long as the maximum amplitude of the input signal E_{sm} is:

$$E_{sm} < \frac{\Delta . f_p}{2\pi f_s} \qquad (1.9)$$

High frequencies of sine wave cannot be encoded by such a system without evoking a slope overload condition unless the amplitude E_{sm} is restricted or the product $\Delta . f_p$ is increased.

Mathematical derivation |4| for a sinusoidal input shows that a linear delta modulator is "completely overloaded" if:

$$E_s = 1.86 \frac{\Delta f_p}{2\pi f_s} \qquad (1.10)$$

In this case the output of the encoder is a sequence of consecutive of one's and zero's at the same frequency as the input signal. The local decoded signal has a step-wise triangular waveform at a frequency again equal to the input sinusoidal signal. Its amplitude will be |4|:

$$E_\Delta = 0.844\ E_s \qquad (1.11)$$

During an overloading condition the signal at the output of the decoder will be very different from the original signal. The input to the low-pass filter is a triangular waveform instead of a close approximation of the input signal. Fourier analysis of this signal shows that the decoded signal will contain odd harmonics of the

fundamental input f_s in a trigonometric series. These harmonics will cause a noise known as "slope overload noise", which is generally much larger than the quantization noise.

Threshold of coding is defined by the lower limit of the input signal to an encoder which just disturbs the idling pattern of the encoder |8|. If the amplitude of the input signal E_s is smaller or equal to $\Delta/2$, then the encoder is incapable of tracking the input signal and the decoded output will have severe distortion causing a noise known as "amplitude noise". The greater E_s becomes relative to $\Delta/2$, the better is the tracking. The minimum value of E_s which gives an acceptable S/N ratio is clearly subjective choice. The ratio of E_{sm}, which just overloads the encoder to E_{smin} is defined as the dynamic range (DR) of the input. However, the amplitude range (AR) of an encoder is defined as the ratio of E_{sm} to the value which just disturbs the idling pattern (threshold of coding); i.e. $\Delta/2$. In equation form:

$$AR = \frac{E_{sm}}{\Delta/2} \qquad (1.12)$$

Substituting for E_{sm} from equation (1.9), then:

$$AR = \frac{f_p}{\pi f_s} \qquad (1.13)$$

A good design has AR maximized by ensuring that the sampling rate f_p is much greater than the highest frequency to be encoded i.e. $f_p \gg f_s$.

1-3.4 Quantization noise

If a symmetrical delta modulator is correctly tracking the input signal x(t), i.e. without experiencing any slope overload and with inappreciable channel error, then the decoded signal $\hat{x}$ (t) can be represented as the sum of x(t) and an unwanted signal. This unwanted signal is referred as "quantization" or "granular noise" originating in the encoding process due to the existance of the error signal e(t). The value of e(t) must be small if $\hat{x}$ (t) is to be a close facsimile of x(t), but cannot be zero for the delta modulator to function. In practice, no quantizer can produce an instantaneous change in the vicinity of zero, the change is gradual and consequently the error must be large enough to produce either +V or -V at the quantizer output.

Different definitions of quantization noise are given in literature relating to DM systems [3,4,8].

1- Quantization noise is the signal which occurs when e(t) is passed through the output filter F_o. It is the component of e(t) which is in the message band.

2- Quantization noise is e(t).

It may be noted that definition (1) gives the lowest value of quantization noise and definition (2) yields higher values of quantization noise, as the noise has not been band limited by filter F_o.

The quantization noise power N_q in LDM system can be expressed by |4|:

$$N_q^2 = \frac{K_q \ f_c . \Delta^2}{f_p} \qquad (1.14)$$

Where f_c is the bandwidth of the input signal and K_q is a constant of proportionality and is equal to 1/3 for good encoding.

This value of 1/3 is valid for a limited range, because K_q is constant only over a restricted range of f_c, f_p, and Δ.

Signal to quantization noise ratio is defined by the ratio of the input signal power S to the decoded noise power N_q in the presence of the decoded signal i.e.:

$$s.q.n.r. = \left(\frac{S}{N_q}\right) \qquad (1.15)$$

For sinusoidal input, where E_s is the amplitude of the input signal and $\sqrt{E_s^2/2}$ is the value of its power, then:

$$s.q.n.r. = \frac{1}{\sqrt{2K_q}} \cdot \left(\frac{f_p}{f_c}\right)^{1/2} \cdot \frac{E_s}{\Delta} \qquad (1.16)$$

As the noise power is substantially independent of the signal power S, the s.q.n.r. increases linearly with increasing S and has a peak value when $S = \sqrt{E_{sm}^2/2}$, then the peak value qf s.q.n.r. is, in DB:

$$s.q.n.r.\Big|_{peak} = 20 \log. \left[\frac{1}{\pi\sqrt{8K_q}} \cdot \frac{f_p^{3/2}}{f_s . \ f_c^{1/2}} \right] \qquad (1.17)$$

The above equation shows, from the exponents, signal-to-noise ratio decreases at a rate of 6db/octave with the increase of signal frequency f_s and at a rate of 3db/octave with the increase of the bandwidth of the input signal f_c. Also, it increases at a rate of 9db/octave with the increase of the sampling rate f_p.

When E_s exceeds E_{sm}, the encoder becomes overloaded and the noise power increases by a greater amount than the increase in signal power. This leads to a decrease in the signal to noise ratio. There is only one value of E_s;i.e. when $E_s = E_{sm}$ for which S/N is maximum.

At the threshold of coding the input signal E_s is equal to $\Delta/2$, then the mean square value of the input signal in $\frac{\Delta^2}{8}$. Therefore at the threshold of coding the s.q.n.r. is in dB:

$$s.q.n.r.\Big|_{threshold} = 20 \log \frac{1}{\sqrt{8K_q}} \cdot \sqrt{\frac{f_p}{f_c}} \qquad (1.18)$$

Thus the S/N at threshold will be dependent on the ratio of the bit rate to the signal bandwidth.

CHAPTER - 2

LITERATURE REVIEW

2-1 Introduction

The development of delta modulation (DM) is a comparatively recent pursuit. H.R. Schindler |1| stated that, the basic principles were first described by Deloraine, Van Miero and Derajavitch in a French patent dated in August 1946. Since the early 1950's, more intense attention was given to the subject and detailed aspects of the system were published. A number of these published papers are reviewed in this chapter. The historical development of DM is summarized in this chapter according to the chart shown in figure 2-1. The chart divides the system into five main areas. These are:

1) Basic principles,
2) Performance improvement techniques,
3) Performance analyses,
4) Implementation,
5) Fields of application.

Each area treats and describes the system from a certain point of view, which if taken together, results in a general review of DM development. The following sections review the various studies performed on the subject according to the sequence given above.

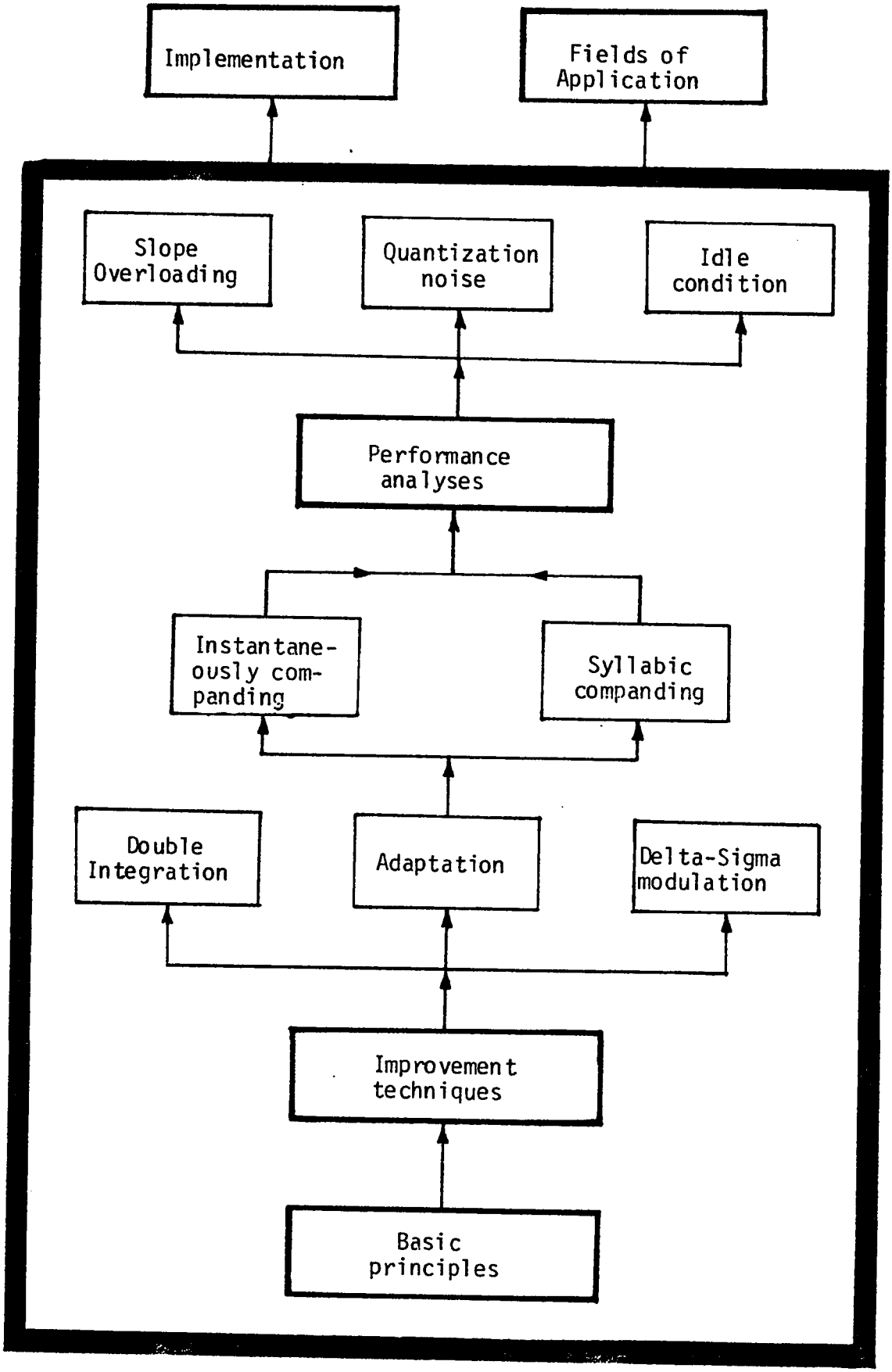


Fig. 2-1 - Various areas of endeavor in d.m. systems.

2-2 Basic Principle of DM System

F. de Jager in 1952 |3| was the first who defined the basic operating principle for delta modulation. He introduced in detail the basic principles for a linear delta modulator; i.e. a system with a single integrator in the feedback loop. The performance of the system, in terms of quantization noise and signal-to-noise ratio, was defined, but without any mathematical derivations. This type of work was repeated by A. Lender and M. Kozouch in 1961 |2| and was a part of the work presented by H.R. Schindler in 1970 |1|, C.J. Kikkert in 1971 |23|, N.S. Jayant in 1974 |21|. More recently, R. Steel in 1975 |4| repeated the work done by De Jager in chapter-1 of his book, but as an introduction to more complicated delta modulation systems.

2-3 Performance Improvement Techniques

As a means to improve the S/N ratio of a linear delta modulation systems, F.de Jager |3| and R. Steel |4| (chapter-2) replaced the single integrator in the feedback loop by a double integrating network as shown in figure 2-2. The predicting resistance (R_p) in figure 2-2 is necessary to minimize the oscillation which results due to the double integration of the digital pattern L(t). They stated also that the time constant R_pC_2 should be small as compared to the time constant R_1C_1 and R_2C_2. Using this method an improvement from 2 to 3 dB in the S/N was gained. Further, H. Inose in

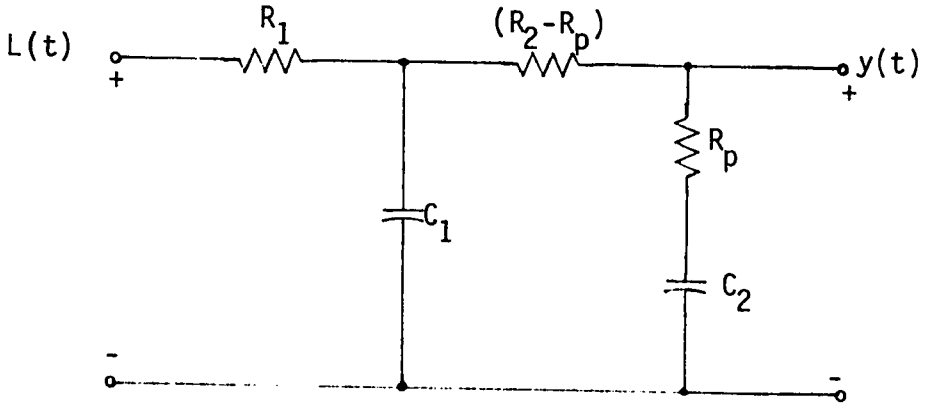


Fig.2-2 - Double integrating network suggested by De Jager and R. Steel to improve the performance of the LDM system.

1963 |29| and R. Steel |4| described delta-sigma-modulation (DSM) system. (Integration of the analogue input is used as the input to the LDM system). They showed that by using such a system, a fixed amplitude of the input signal can be encoded over a wider frequency range than the LDM system. This is because the maximum amplitude of the input signal for the DSM system ($E_{sm} = \Delta.f_p$) does not vary with the signal frequency f_s, as is the case for the LDM system ($2\pi f_s E_{sm} = \Delta.f_p$).

More recently, "companded delta modulation" was described as an additional means to improve the performance of the LDM system. The word companded is composed of (signal dynamic range) compressing at the transmitter and expanding at the receiver. H.R. Schindler |1|

stated that, M.R. Winkler in 1963, was the first who proposed the companding technique to improve the dynamic range of a DM system. His method consists of doubling the size of the quantization step whenever two identical, consecutive binary values appear at the coder output. The step size is divided in half after each transition from one binary level to another. This method is termed "High information DM" (HIDM). Later on J.E. Abate in 1967 |7| described a discrete companding system as a method to obtain adaptive delta modulator. The binary level sequence of the encoder output is observed to control the change of the step size in finite increments. The HIDM system described by Winkler and the discrete companding system described by Abate are grouped under the category of instantaneously companded DM (ICDM) systems. N. S. Jayant in 1971 |19| and in 1974 |21| added a one bit memory element, to the system described by Abate, and defined the companding factors P and Q (see chapter-4) which relate to the step size change. He also showed that in order to maintain stability, the product P.Q. should be always equal to or less than one. R. Steel |4| (chapter-8) also discussed the basic concept of ICDM and described different methods to obtain such companded systems. These include: High Information DM, Discrete Adaptive DM, Statistical DM, etc.

Continuously variable slope delta (CVSD) modulator, or as it is known usually by "digitally controlled" or "syllabically companded" delta modulation, is also used to improve the performance of the LDM system. It is a well-known method to encode speech signals. Again

H.R. Schindler |1| stated that, Greefkes and de Jager in 1968 developed the CVSD concept, where the quantization step is varied continuously. This method was also mentioned by R. Steel |4| (chapter-7). He presented two different methods to obtain the companding information from the digital pattern L(t) at the output of the encoder. The first method is completely analogue, whereas the second method uses digital techniques to detect the slope variation of the input. These two methods are described in detail in chapter-4.

2-4 Performance Analyses

The performance of delta modulation system has been widely investigated by researchers. Many papers were published in this field. These papers analyzed the performance theoretically, as well as practically, and showed that SNR is an useful measure of delta modulation system performance. Parameters such as sampling rate, amplitude and the frequency of the input signal, type of the local decoder single or double integration), and the step size of the reconstructed wave effect the performance of a DM system.

F. de Jager |3|, F.B. Johnson |8|, and R. Steel |4| analyzed the linear DM system and gave mathematical expressions for quantization noise and for SNR in terms of the parameters mentioned above.

J.E. Iwersen in 1969 |30| studied an assymmetrical encoder (an encoder with unequal positive and negative steps). He showed that assymmetry in step can be very advantages in attaining lower

granular (quantization) noise than an encoder with symmetric (equal positive and negative) steps. He also stated that an assymmetrical encoder will distort the idling pattern of the symmetric encoder.

Slope overloading, for a LDM system with sinusoidal input, was discussed in detail by R. Steel (chapter-5) |4|. Expressions for both "just" and "grossly" slope overloading conditions were given in mathematical form. Also the type of the decoded signal under the grossly slope overloading condition was defined.

The idling condition was defined first by Paul P. Wang in 1968 |6|. Basic properties were discussed and using the analytical results, the waveform at the decoder was predicted. J.E. Iwersin |30| indicated that this type of noise results from the unequality of the positive and negative step-size. R. Steel (chapter-6) |4| corroborated the reason given by Iwersin for this type of noise. He predicted the waveform as a saw tooth and gave the expression for its frequency. All three authors stated that this type of noise can be reduced considerably by careful design of the encoder.

Companded DM systems were also analyzed for their general performance. Due to its irregular feedback signal (instantaneous or continuous variation of the step size), direct mathematical analysis is exceedingly more difficult than for a linear delta modulation system. Consequently, most published studies were based on experimental results. Companding factors P and Q, in the instantaneously companded DM systems, syllabic filter time constant, and

shift register length (n) in syllabically companded DM system were optimized upon the subjective choise of the system performance. N.S. Jayant |19| studied the instantaneously companded DM system and defined the dependence of granular (quantization) noise on the adapting factor P. He suggested an optimum value for the companding factor P such that P≈1.5 and the product P.Q <1 to maintain stability of the encoder. He also showed in his paper in 1971 |20| that slope overload distortion exist only in relation to an original input signal. He stated that this type of distortion is not known to the listner and is less annoying than granularity. Furthermore, W. M. Boyee in 1976 |31| examined the response of the system defined by N.S. Jayant |19| for a step function input signal. He defined a new integer n and showed that the system is stable only when the product $P^n.Q<1$ for all initial conditions.

Papers published in the performance analyses of the syllabic companded system are very few. Nearly all the reviewed papers; i.e. articles published by R. Steel |4,5|, Don Johnson |11|, and T.S. Lamba |22| define the basic principles of the (SCDM) system. No clear justification of the performance of the system was given in terms of the syllabic filter time constant,shift register length (n) in the SSA network, loop gain and the sampling rate. They just indicated that for speech encoding the suitable range of the syllabic filter time constant is from 4m sec to 10m sec.

This thesis, considers this type of the companded delta modulation system built as integrated circuit by two different manufacturers. The performance of the system in terms of the syllabic filter time constant, shift register length (n), loop gain and the sampling rate f_p is discussed with detail in chapters 5 and 6.

2-5 Implementation of DM Systems

Reviews of papers since the 1950's reveal that as technology advanced, it was possible to implement the DM system in simpler forms and with lower cost. R.B. Wattson and O.H. Hudson in 1956 |32| used vacuum tubes, whereas B.E. William in 1959 |9| used junction transistors and their associated external components to implement linear delta modulation systems. R. Steel and M.W.S.Thomas in 1968 |10| used a monostable element in the forward path of the encoder and on RC network as the local decoder. They also described an encoder using a bistable element in the forward path. H.R. Schindler in 1970 |1| and John A. Betts in 1971 |33| used digital logic gates, flip flops, and shift registers built as integrated circuits to implement adaptive delta modulators. Don Jones in 1978 |11| presented a linear DM system and a (CVSD) modulation system using operational amplifiers, together with D-type flip-flop and shift registers.

More recently, several manufacturers such as Motorola Semiconductor |25| , Harris Corporation |26|,and Microcircuits of America |5| had produced a single chip of (CVSD) modulation system costing

only few dollars. These chips were also mentioned by J. H. Kelly, J. J. Price in April 1977 |24|, R. Steel in October 1977 |5| and Don Johnson in January 1978 |11|.

2-6 Fields of Application

Excluding the application of DM systems for encoding speech and video signals, authors showed that it is possible to use DM systems for other purposes too. J.C. Balder and C. Kramer in 1964 |34| and Toshihiko Y. Taikyukim in 1978 |35| discussed in detail the possibilities of encoding DC signals using DM systems. J.B. O'Neal in 1974 |36| described the use of DM system for data transmission. D.J.G. Janssen in 1972 |37| presented a digital voltmeter using DM system. Its application in other measuring instruments, digital filters, and in remote control was also described by R. Steel |4,5|.

Chapter - 3

PRACTICAL INVESTIGATION OF AN LDM SYSTEM

3-1. Introduction

As part of the investigation of delta modulation, an LDM system has been designed, breadboarded, and tested. Fig. 3-1 shows a block diagram of a linear delta modulator corresponding to the one constructed. Various techniques have been proposed by different authors to implement the above system [9,10,11]. The approach to implement this system, which functions according to the theory stated in Chapter 1, is shown in fig. 3-2.

3-2. System Description

The function of the comparator and the quantizer, of fig. 3-2, is combined in a high gain differential amplifier. Two (AND) gates operating one on the positive logic and the other on the negative logic are needed to sample the quantizer output at a constant clock rate f_p. An output "adder" is also required to superimpose the two AND gates output. The integrator in the feedback loop converts the digital pulses into step-like waveform which approximates the input x(t).

To eliminate the need of an AND gate operating in negative logic, an alternate system was used having a combination of a second positive logic AND gate, preceded and followed by inverting circuits. This combination functions as a negative logic AND gate. The inverter preceding the AND gate provides a positive level for

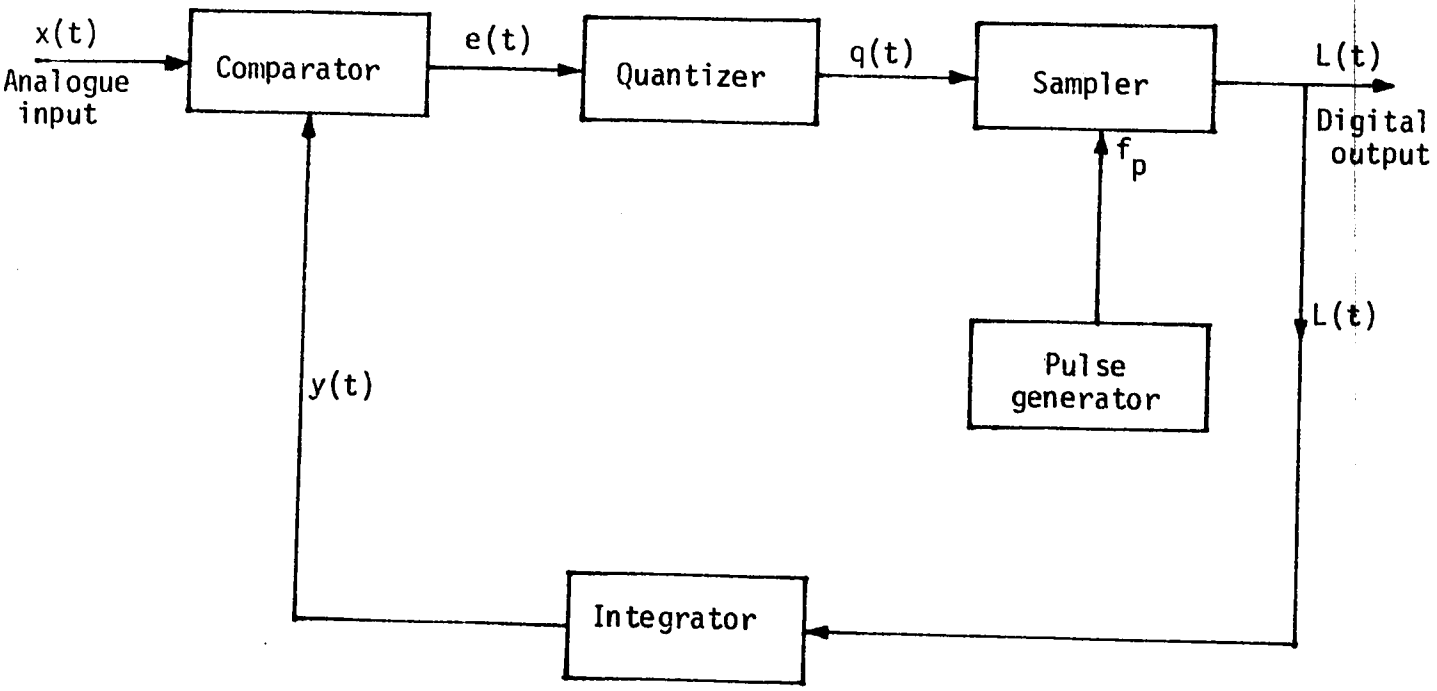


Fig. 3-1 - Block diagram of a linear delta modulator.

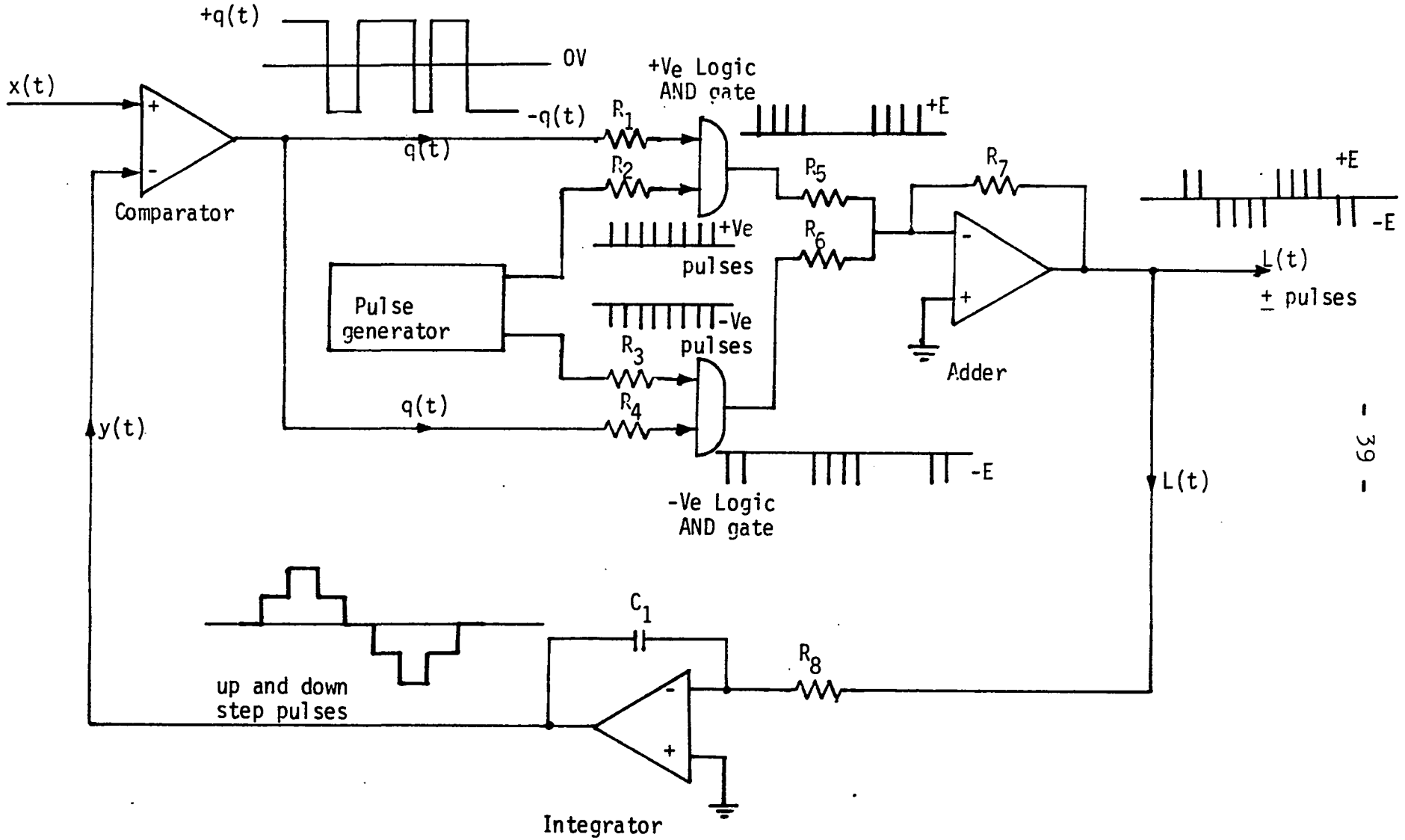


Fig. 3-2 - Schematic diagram of the linear delta modulator.

sampling by the AND gate. The sampled pulses are then reinverted to their original negative direction, by the second inverter. Fig. 3-3, shows the modified circuitry of the linear delta modulator.

The analogue input signal x(t), and the integrated feedback signal y(t) are compared by the comparator. The output of the comparator saturates at either a positive or a negative value, depending on the sign of net input signal e(t). Both levels are sampled at a constant sampling rate f_p. The positive level is sampled by the first positive logic AND gate, whereas the negative level is sampled by the combination acting as a negative logic AND gate. The output of the two AND gates are added together to form the delta modulated signal L(t), which is a train of pulses that may have either positive or negative values.

3-3. System Design

Generally, the performance of a delta modulator is described by the signal to noise ratio, bandwidth and the dynamic range of the input signal. The most important parameters controlling the performance of a LDM system are the sampling rate f_p and the loop gain, which in turn controls the step size Δ of the feedback signal. Different sampling rates and different step sizes lead to different characteristics. In order to implement a LDM system which will be comparable with those implemented on integrated circuits (CVSD systems devices of Motorala and Harris), a sampling rate of 16 KHZ and

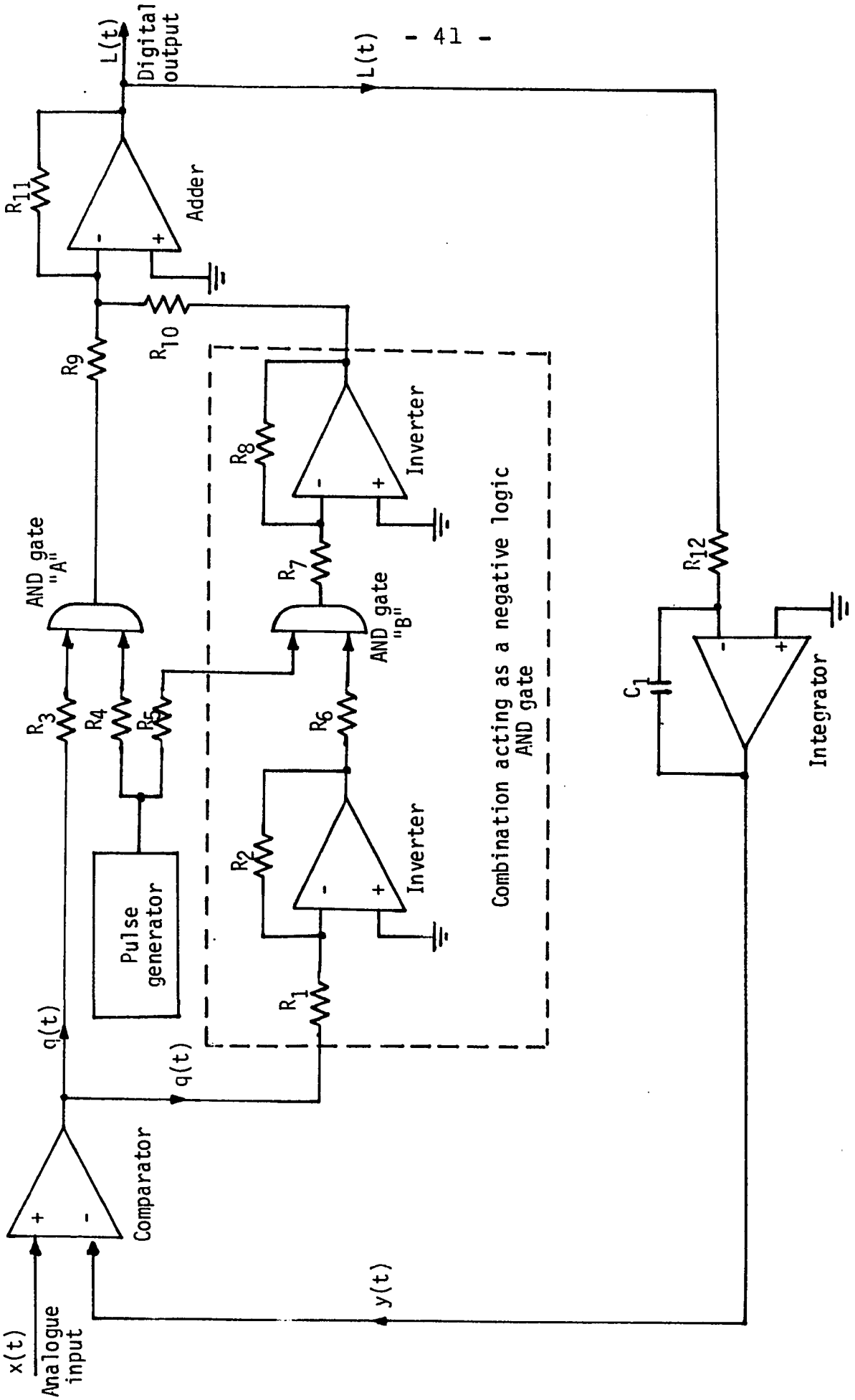


Fig. 3-3 - Modified schematic diagram of the linear delta modulator.

step size of 120 mV are incorporated in design requirements. This choise of parameters is to have both systems at identical operating condition.

In constructing the circuitry of the linear delta modulator shown in fig. 3-3, discrete components interconnected by the conventional technique were avoided as much as possible. The technology of integrated circuits offers a number of advantages, such as:

* Space occupation is small,
* Designing procedure is simplified,
* The system operation is easier to follow,
* The overall performance is generally better,
* Offers high reliability and faults can be remedied more quickly,
* The cost and fabrication time is reduced considerably.

The various configurations of linear operational amplifiers and the digital integrated logic circuits were found to be of great help in satisfying the theory of LDM systems |12,13|. Figure 3-4 shows the schematic diagram of the linear delta modulator as it exists in hardware. Waveforms, at different test points allocated on the system, are shown in the various photographs. These photos were taken with a sinusoidal input and grossly slope overloading the system. Figure 3-5 shows the digital pattern consisting of consecutive numbers of one's and then zero's at a repetition rate equal to that of the input signal, and its integration to a stepwise triangular wave. Fig. 3- 6, shows the comparator output having a rectangular

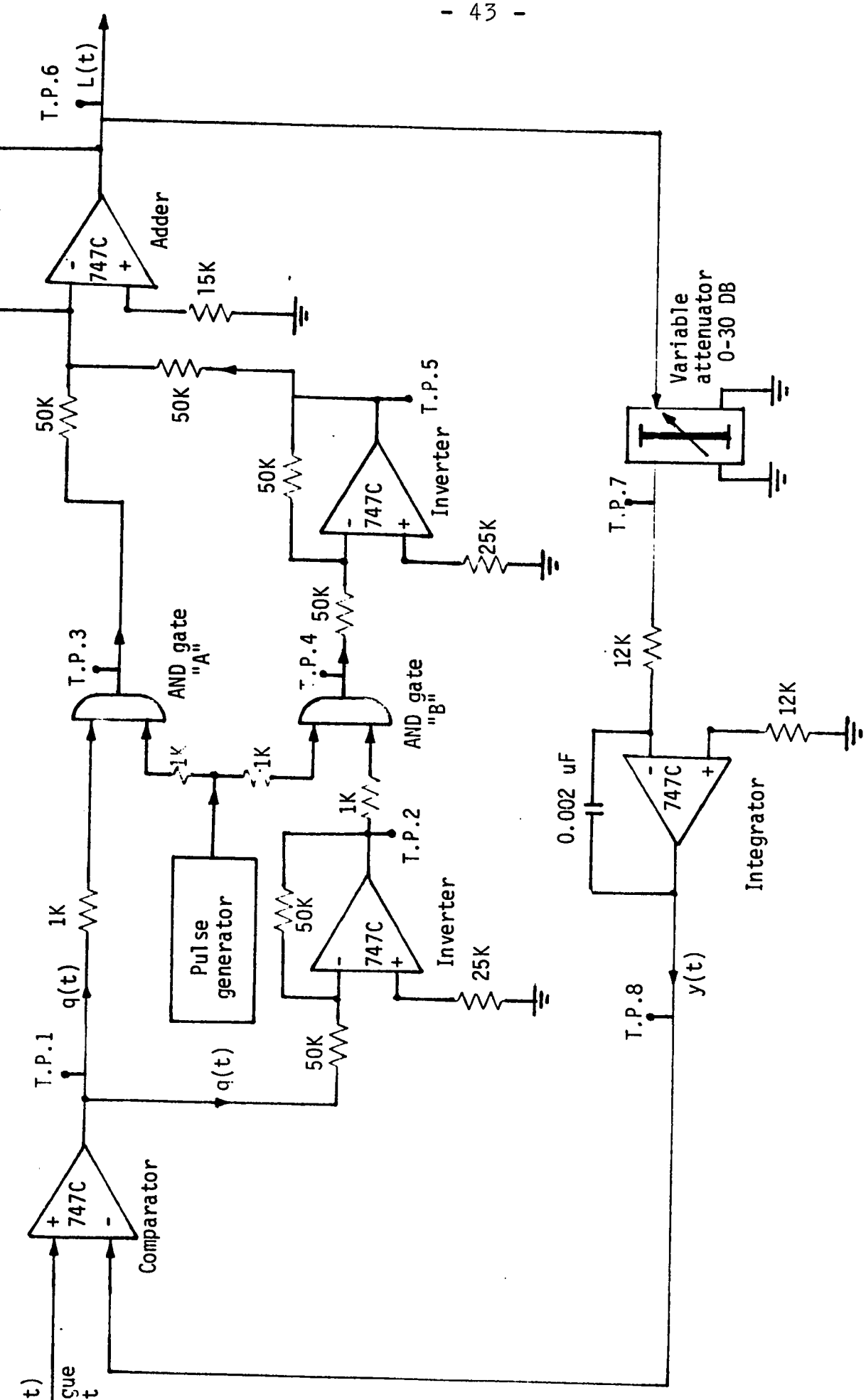
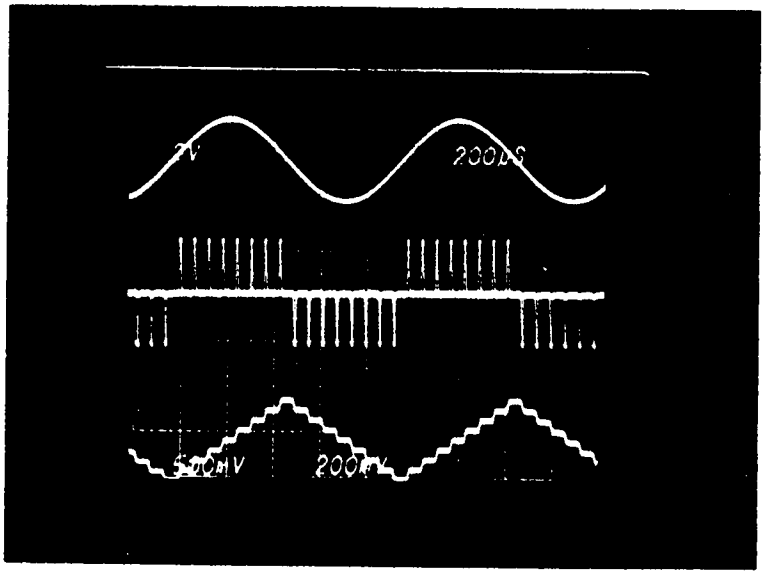


Fig. 3-4 - Linear delta modulator as exist in hardware.

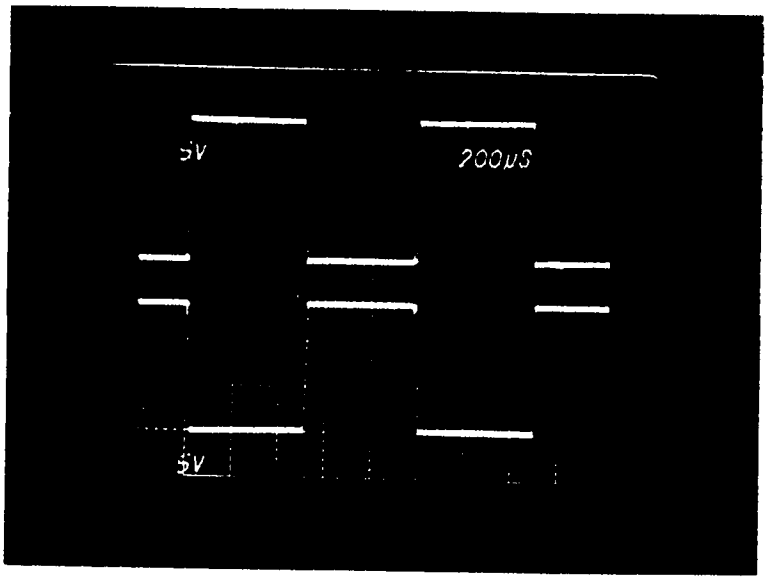


Analogue input 4V p-p, at 1000 HZ.

Digital input to the integrator ± 220 mv at T.P.7.

Reconstructed wave at T.P.8.

Fig. 3-5 - Waveforms at the input and the output of the encoder, system in slope overloading condition.

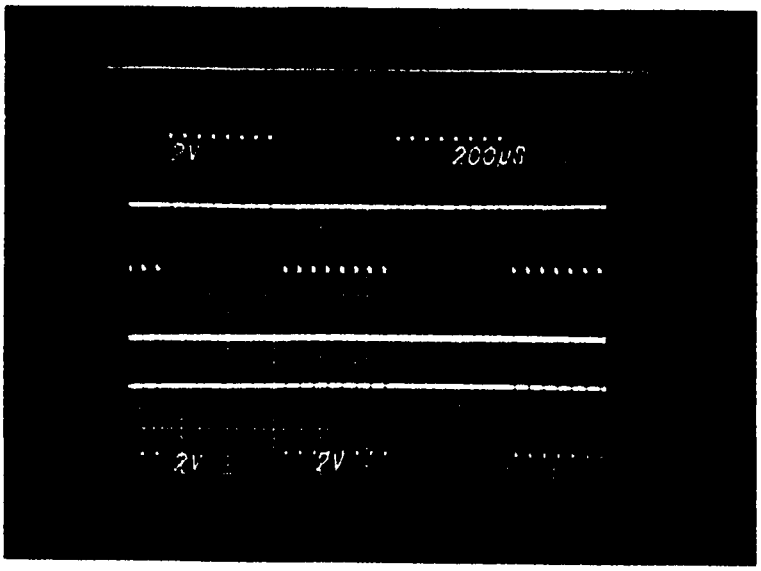


Comparator output at T.P.1, 16.0V p-p.

Comparator output at T.P.2, after inversion, 16.0V p-p.

Fig. 3- 6 - Quantized signal at the output of the comparator.

shape at a freauency equal to that of the input signal. This is because, in the overloaded condition, the error signal e(t) is positive during the rising period of the triangular wave, and is negative during the falling period. Both rising and falling times are equal since the number of one's and zero's generated at the output of the encoder are equal. Fig. 3-7, shows the sampled waveform at the output of the AND gates. This photograph shows that when AND gate A is at high level, gate B is at low level and vice versa. The speed of operating the AND gates is controlled by the sampling rate f_p.



output of AND gate "A" at T.P.3, + 3.0V.

output of AND gate "B" at T.P.4, + 3.0V.

output of AND gate "B" at T.P.5, after inversion, -3.0V.

Fig. 3-7 - Sampled waveform at the output of the sampling AND gates.

3-4. System Testing

The constructed linear delta modulator has been tested at the following operating conditions:

1) Idling condition,

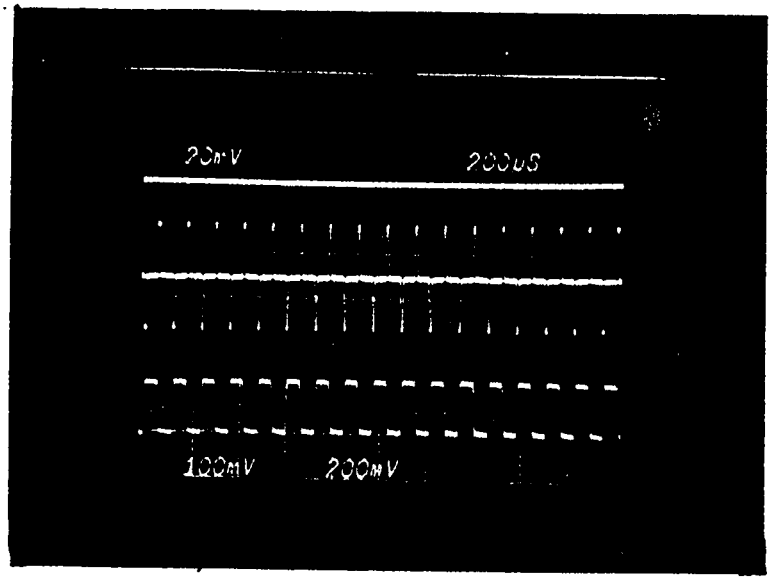
2) Normal operating condition,

3) Slope overloading condition.

The purposes of the above tests are to evaluate the performance of the system, as well as to show that the implemented system satisfies the theory of a LDM system. Waveforms obtained at each operating mode will be discussed to compare with those shown in chapter one. The overall performance of the system was determined by frequency response and quantization noise measurements. These measurement results are compared with those theoritically expected.

3-4.1 Idling operation

Usually a delta modulation system is in its idling state, when there is no input signal. The response of the constructed LDM system at this condition (fig. 3-8) shows a pattern similar to that of a symmetrical encoder; i.e. a sequence of one's and zero's. Fig. 3-9 , illustrates this idling pattern in more detail. The waveform at the output of the local decoder looks like a trapezoidal wave, with a peak-to-peak amplitude of 120 mV, i.e. the value of the step size Δ. The frequency of the digital pattern L(t) and of the reconstructed waveform y(t) is 8 KHZ, which is

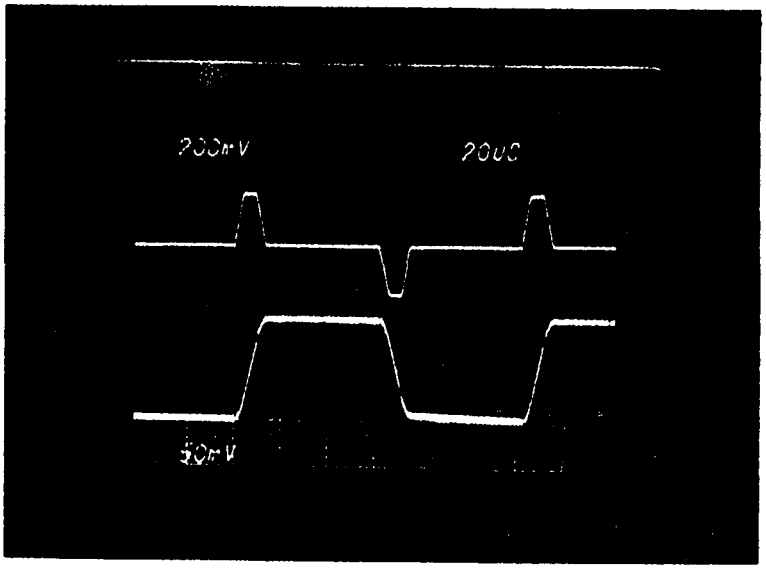


a) Analogue input x(t)
0.0 volt.

b) Digital output L(t), at idling.

c) Reconstruct waveform y(t), at idling.

Fig. 3-8 - Idling pattern of the LDM system.



a) Digital output L(t)
$\pm$ 220 mv, 8 KHZ.

b) Reconstructed waveform y(t), 8 KHZ, 120 mv p-p,

Fig. 3-9 - Idling pattern of the LDM system (Magnified in time).

one half the value of the sampling rate f_p. Generally, at idling:

$$f_L = f_y = f_p/2 \qquad (3\text{-}1)$$

This is because two sampling pulses are needed to generate a sequence of one and zero at the output of the encoder.

The frequency spectrum of the y(t) waveform, shown in figure 3-9 , consists of predominent components at the half the sampling rate and its odd multiples (figure 3-10). Smaller peaks at the even multiples of $f_p/2$ also exists (figure 3-11). These peaks (odds and even) are correlated to the frequency spectrum of an assymmetric trapezoidal waveform. A graphical approach may illustrate that a symmetrical periodical waveform contains only odd harmonics in its frequency spectrum. Even harmonic may also exist if the waveform has assymmetry in its rising and falling time periods. This was verified graphically in figure 3-12 and 3-13 for a symmetrical and assymmetrical trapezoidal waveform respectively. Generally a function $f(\theta)$ can be broken into its even and odd harmonics by writing a function $f(\theta)$ as follows:

$$f(\theta) = \tfrac{1}{2}\left[f(\theta) + f(\theta+\pi)\right] + \tfrac{1}{2}\left[f(\theta) - f(\theta+\pi)\right] \qquad (3\text{-}2)$$

The preceding equation can be easily verified by performing the algebra indicated on the right-hand side.

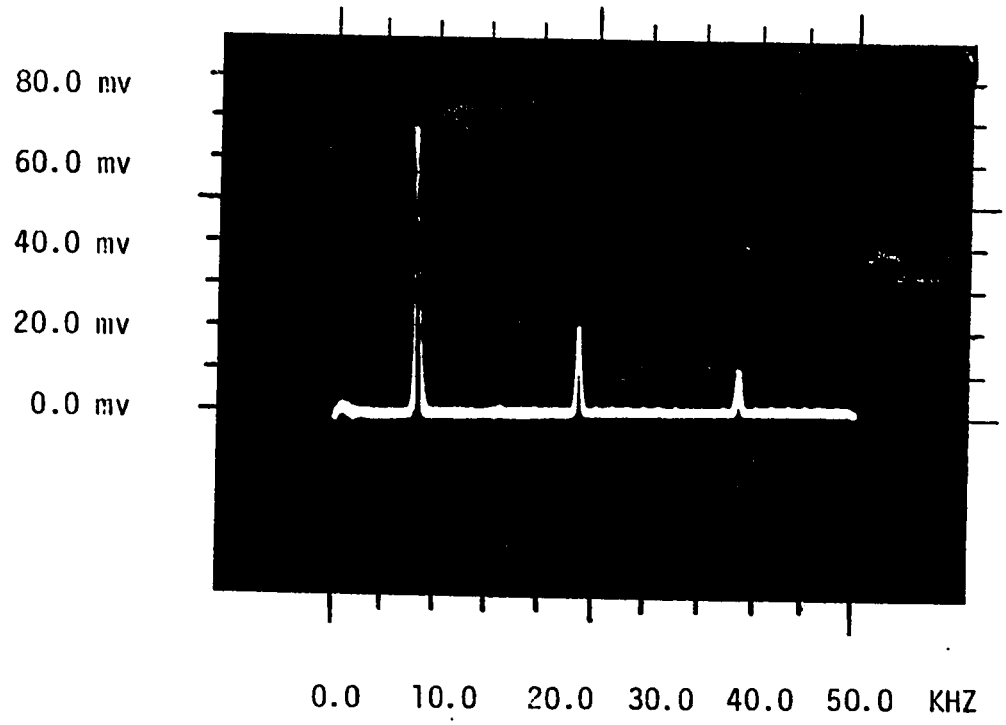


Fig.3-10 Frequency spectrum of locally decoded waveform at idling.

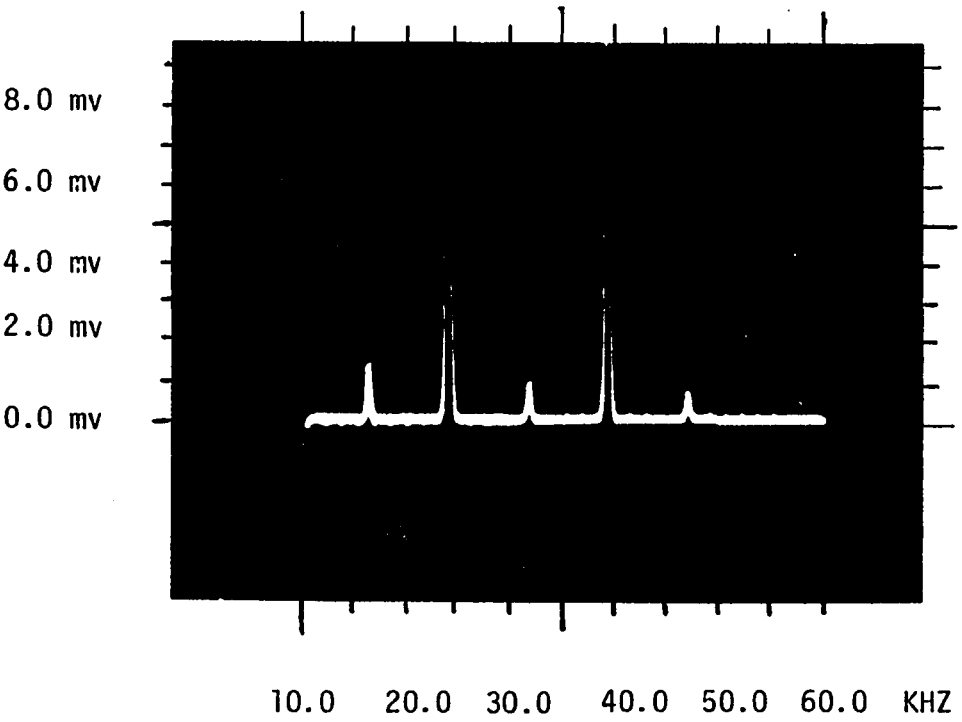


Fig. 3-11 Frequency spectrum of the locally decoded waveform at idling showing the even peaks.

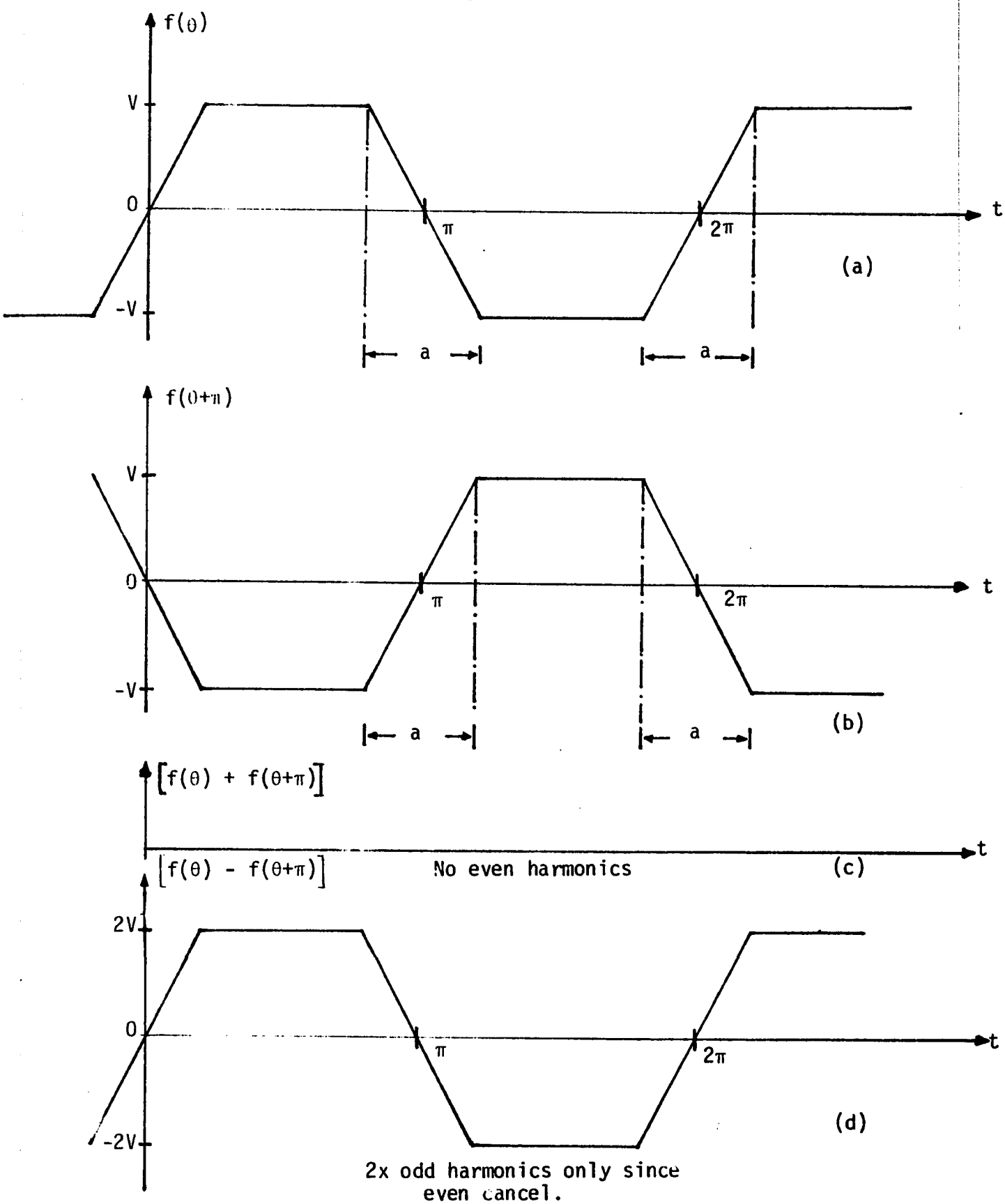


Fig. 3-12 - Graphical approach to show that only odd harmonics exist in the spectrum of a symmetrical trapezoidal wave.

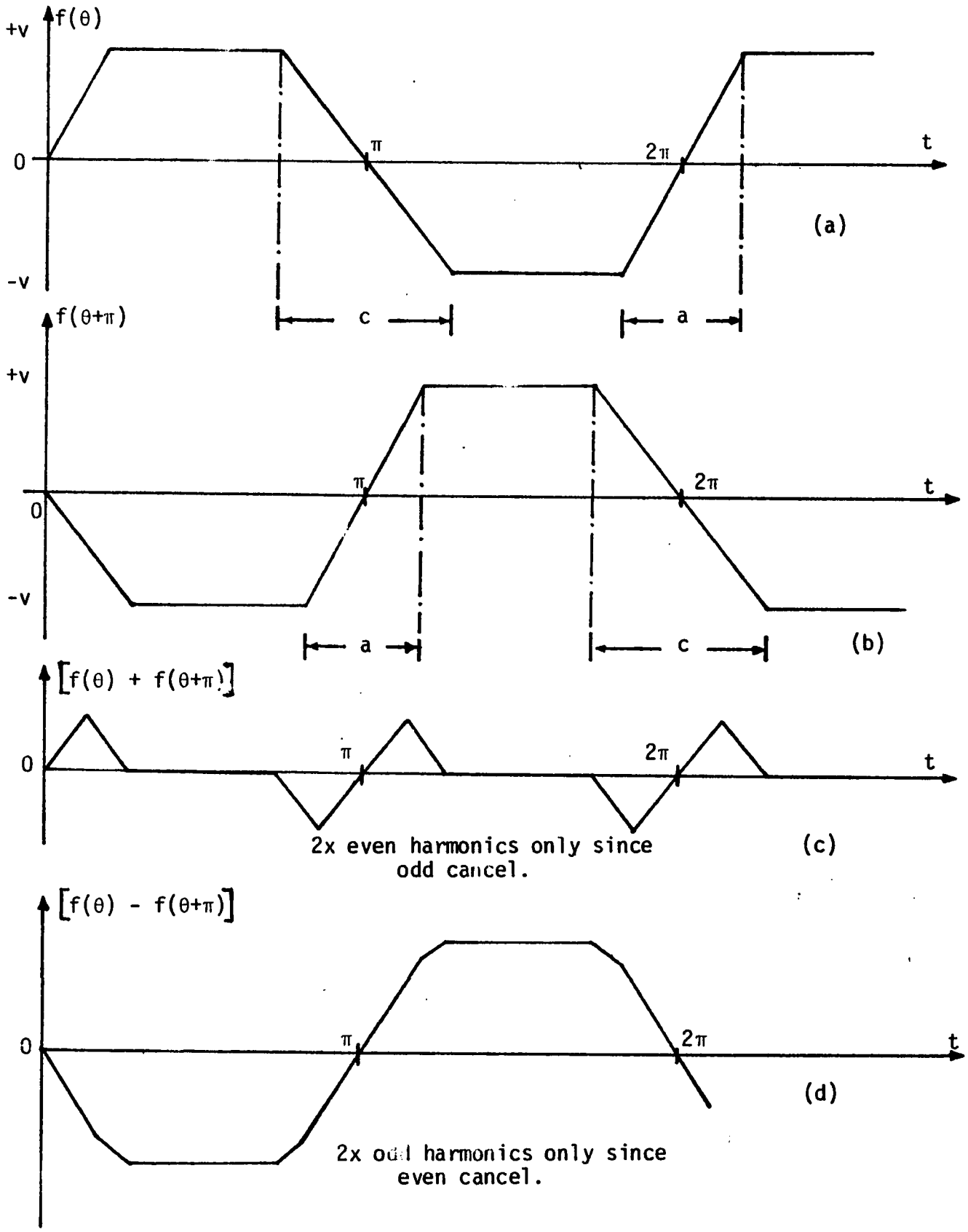


Fig. 3-13. Graphical approach to show that both even and odd harmonics exist in the spectrum of an assymetrical trapezoidal wave.

The Fourier expansion of an assymmetrical trapezoidal waveform is as follows [appendix-1]:

$$f(t) = \frac{a_o}{2} + \sum_{n=1}^{\infty} C_n \, Cos(nwt + \phi_n) \qquad (3\text{-}3)$$

Where: $C_n = \sqrt{a_n^2 + b_n^2}$, $\phi_n = \tan^{-1} \frac{a_n}{b_n}$ (3-4)

And: $a_o = \frac{A}{\pi} (c - a)$ (3-5)

$$a_n = \frac{2A}{\pi n^2} \left[\frac{1}{a} (Cos\ na + \frac{na}{2} Sin\ na - 1) - \frac{1}{C} Cos\ n\pi \{Cos\ nc + \frac{nc}{2} Sin\ nc - 1\} \right] + \frac{A}{n\pi} \left[Cos\ n\pi\ Sin\ nc - Sin\ na \right] \qquad (3\text{-}6)$$

$$b_n = \frac{2A}{\pi n^2} \left[\frac{1}{a} \{Sin\ na - \frac{na}{2} (Cos\ na + 1)\} - \frac{1}{C} Cos\ n\pi \{Sin\ nc - \frac{nc}{2} (Cos\ nc + 1)\} \right] - \frac{A}{n\pi} \left[Cos\ n\pi (1 + Cos\ nc) - (Cos\ na + 1) \right] \qquad (3\text{-}7)$$

Where a and c are the total rising and falling time periods, respectively. Evaluated from figure 3-21, a = 12 μsec or 0.192π radians, C = 10.0 μsec or 0.16π radians The first six peaks were computed using equations 3-4 , 3-6 and 3-7. The error between the computed and the measured peaks in table 3-1 is mainly due to the difficulty of the accurate estimation of the factors a and c from figure 3-9 . The amplitudes of the even peaks depends upon the amount of assymmetry existing in the waveform. It is higher with greater assymmetry and vice versa. A precise design procedure is required to obtain a symmetrical trapezoidal wave at idling, to eliminate the presence of the

No. of peak	Measured values		Computed Amplitudes mv	% Difference	Relative amplitude w.r.t. the fundamental
	Amplitude mv	Frequency KHZ			
1st	70.0	8.0	75.40	7.0	100 %
2nd	1.5	16.0	1.86	19.0	2.0 %
3rd	22.0	24.0	22.56	2.5	31.0 %
4th	1.0	32.0	1.67	40.0	1.4 %
5th	12.0	40.0	10.75	-11.6	17.0 %
6th	0.8	48.0	1.08	26.0	1.1 %

Table 3-1 - Measured and computed peaks of the decoded wave at idling condition.

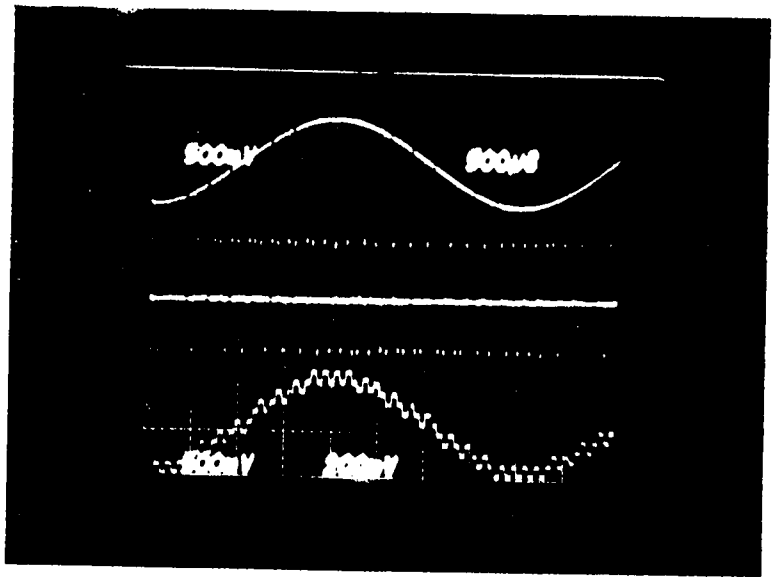
even peaks. However, the existance of the odd and the even peak is not troublesome since a low-pass filter at the output of the decoder attenuates these peaks to a negligible amount.

3-4.2 Normal operation

It was previously indicated that the linear delta modulator has amplitude bounds on the input signal to operate in the normal condition. The maximum limit was given by equation 1-9 and the minimum bound was given by threshold of coding; i.e. $\Delta/2$. Mathematically, the limits of E_s for normal operation can be rewritten using equation 1-9 and the defination of the threshold of coding as:

$$\frac{\Delta}{2} < E_s < \frac{\Delta . f_p}{2\pi f_s} \qquad (3\text{-}8)$$

In normal operation, the encoder is able to track the input within an error not more than Δ. The system is said to be slope overloaded if the error exceeds Δ, where two or more steps are required to achieve the input value. A sinusoidal signal with an amplitude and frequency satisfying the condition given by equation 3-1 was selected as the input to the modulator. Figure 3-14a shows an input condition for which the LDM system functions normally. Usually, in the normal operating condition, the stepwise approximation of the input has slightly larger peak-to-peak excursion values (Figure 3-15). At the maxima and the minima, where the slope tends to be zero, the reconstructed wave has a sequence of one's and zero's. By applying this



a) Analogue input x(t), 1.0V p-p at 250 HZ.

b) Digital pattern L(t).

c) Locally decoded waveform y(t).

Fig. 3-14 - Linear delta modulator's waveforms in normal operation.

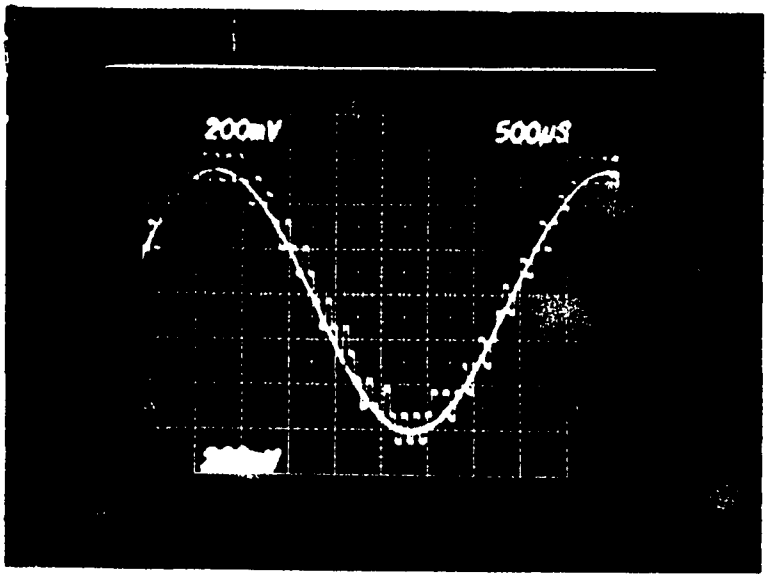


Fig. 3-15 - Step wise approximation of a sinusoidal signal at normal condition.

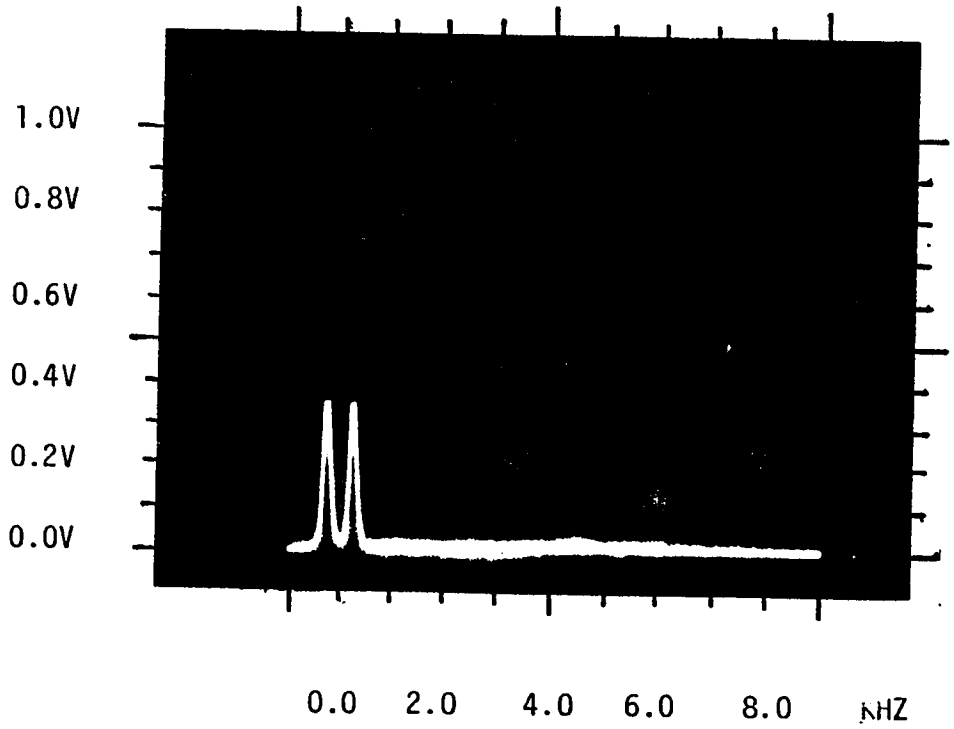


Fig. 3-16 - Locally decoded waveform as displayed by the spectrum analyzer.

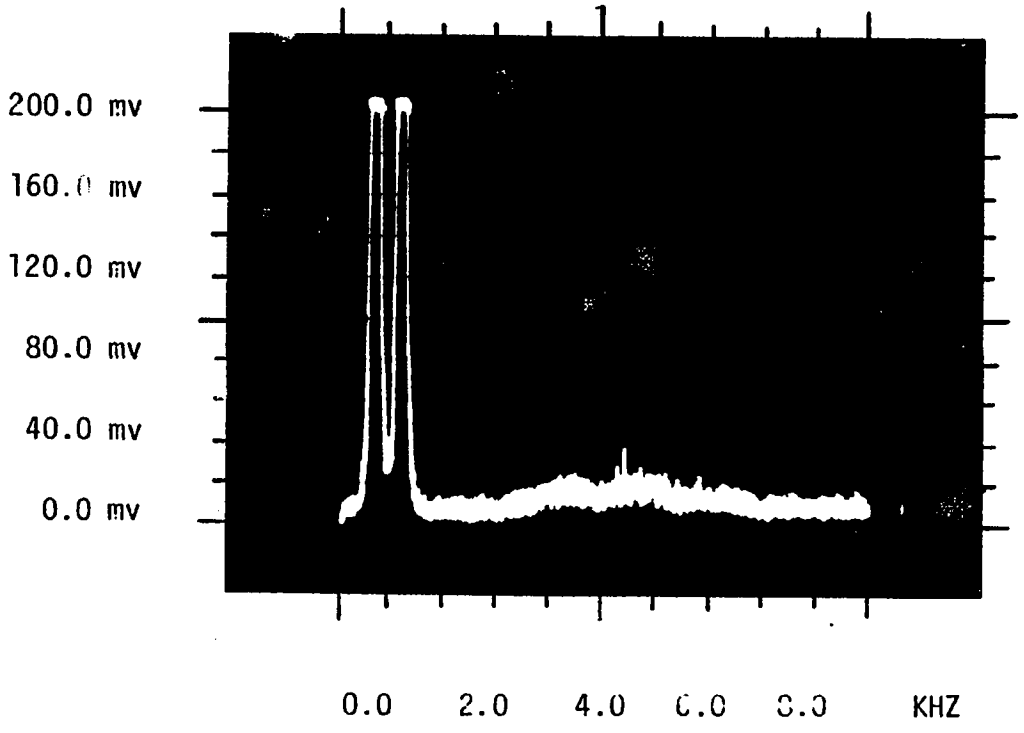


Fig. 3-17 - Frequency spectrum display of the locally decoded waveform showing the quantization noise at sampling rate f_p = 16.0 KHZ.

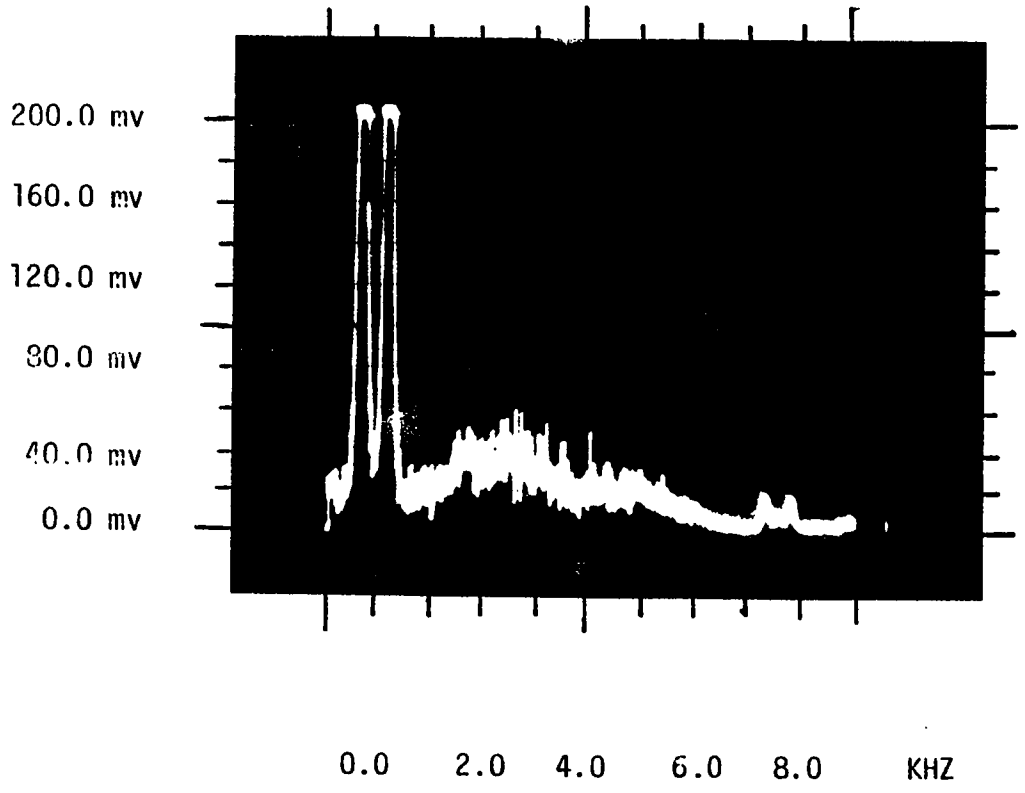


Fig. 3-18 - Frequency spectrum of the locally decoded waveform showing the quantization noise at sampling rate f_p=8.0 KHZ.

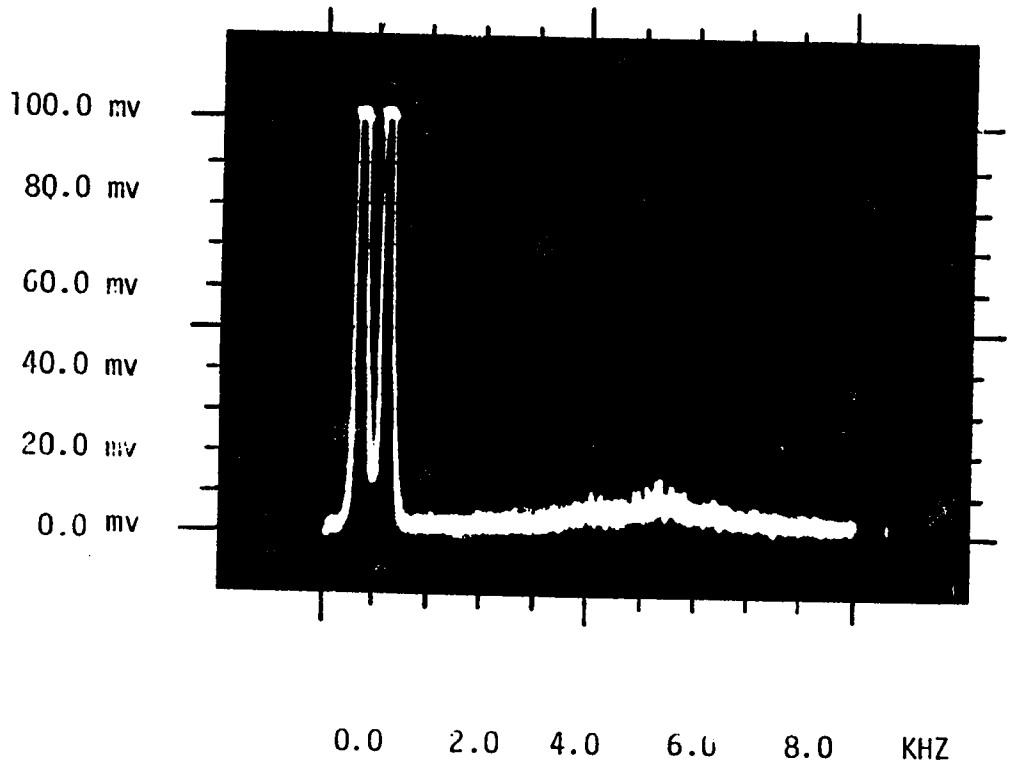


Fig. 3-19 - Frequency spectrum of the locally decoded waveform showing the quantization noise at sampling rate f_p = 32.0 KHZ.

wave to a low-pass filter, the error between the input and the recovered signals are appreciably reduced.

A spectrum analysis of the locally decoded waveform (Figure 3-16) shows two peaks at $\pm$ 250 HZ (the frequency of the input signal) and a relatively small noise level. This level is shown more vividly in figure 3-17. A peak value of 24.0 mv occurs in the band from 3.0 KHZ to 6.0 KHZ. By sampling the same input signal, once at half the 16.0 KHZ and once at twice the 16.0 KHZ (Figures 3-18 and 3-19), the noise level was found to be higher at lower sampling rates.

The overall distribution of the noise over a band equalling the sampling rate is not uniform and also appears to occur in various levels at discrete frequencies. Figures 3-17 - 3-19, show the noise over a total display width of 9.0 KHZ (1.KHZ per division). These figures indicate that it is impossible to measure the separation Δf between consecutive discrete frequencies. Figures 3-20 is useful for determining how power (energy) can be computed from the spectrum analyzer data. It shows a schematic amplitude distribution of a function $A(F_i)$ at discrete frequencies, spaced by Δf. Having Δf grow smaller (Figure 3-40a)requires $A(f_i)$ to decrease, if the energy is to remain the same. In the limit the ratio $\frac{A(f_i)}{\Delta f}$ versus the frequency must be considered to evaluate energy for the continuous function $\frac{dA(f_i)}{d_f}$ (Figure 3-40b). The energy content within a certain bandwidth $f_c = (f_b - f_a)$ is given by |17|:

$$W_{ab} = \int_{f_a}^{f_b} \left[\dot{A}(f_i)\right]^2 \, d_f \qquad (3\text{-}9)$$

Where: $\dot{A}(f)$ is $\frac{dA(f_i)}{d_f}$ (spectral density)

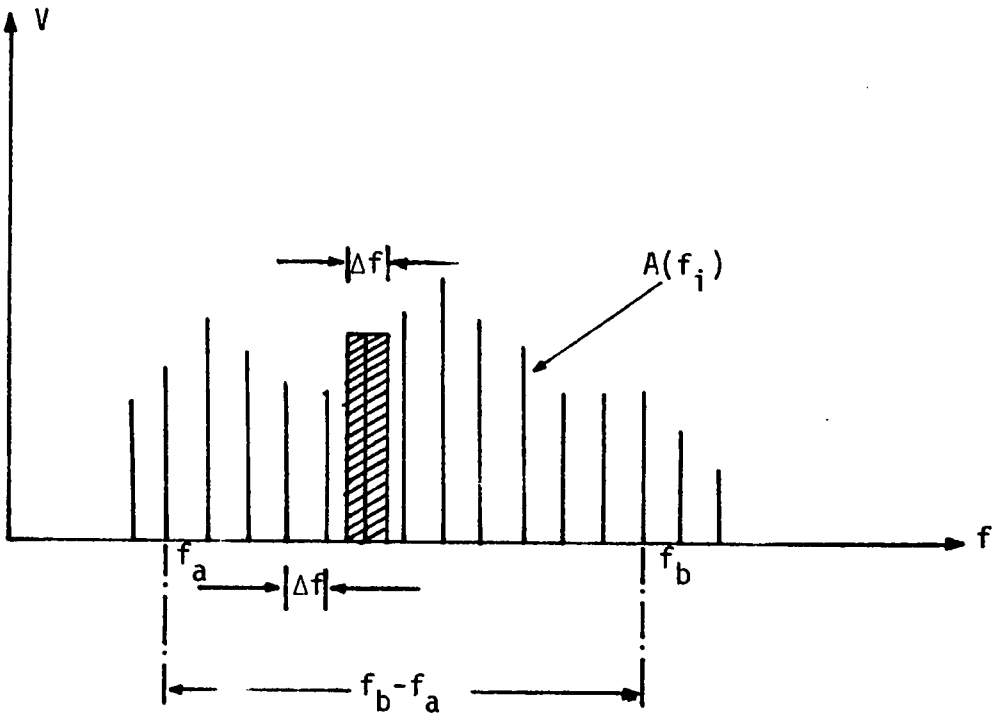


Fig. 3-20 - Distribution of a function $A(f_i)$ at discrete frequencies.

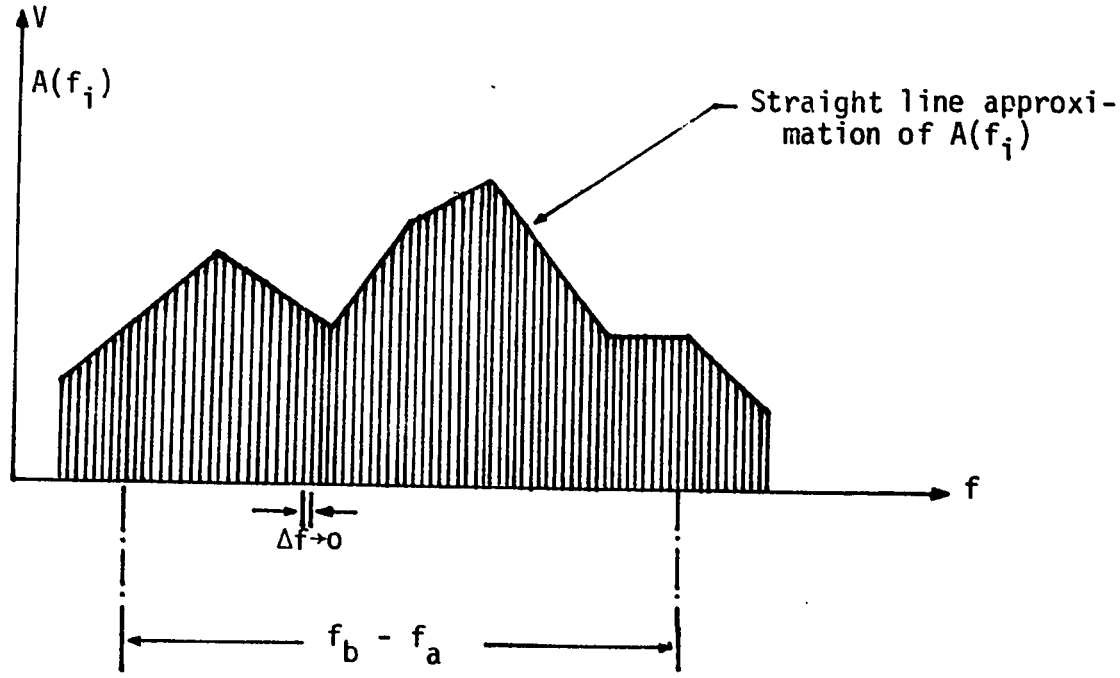


Fig. 3-21a - Distribution of the function $A(f_i)$ for small Δf.

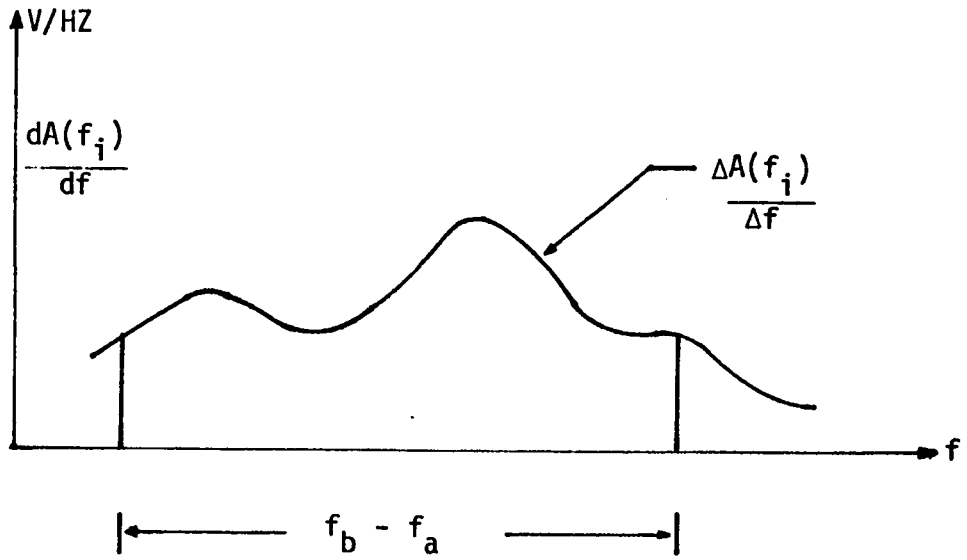


Fig. 3-21b - Spectral density $\frac{dA(f_i)}{df}$ plot.

The energy given by equation 3-9 should be equal to that from a summation of the discrete energies of the function shown in figure 3-20 (spectrum analyzer display) within the same bandwidth f_c; i.e.

$$W_{ab} = \sum_{f_a}^{f_b} \frac{|A(f_i)|^2}{\Delta f} \qquad (3\text{-}10)$$

Rewriting equation (3-10) as:

$$W_{ab} = \sum_{f_a}^{f_b} \frac{|A(f_i)|^2}{\Delta f} \cdot \frac{\Delta f}{\Delta f} = \frac{1}{\Delta f^2} \sum_{f_a}^{f_b} |A(f_i)|^2 \, \Delta f$$

For sufficiently small Δf:

$$W_{ab} = A/\Delta f^2 \qquad (3\text{-}11)$$

Where: A represents the total area of the displayed amplitude envelope squared, within the bandwidth $f_c=f_b-f_a$ To obtain an approximate evaluation of the energy content within a certain bandwidth f_c, the envelope of function $A(f_i)$ (Figure 3-21) is squared and its area is then computed. For convenience, straight line segments are used between the peak levels.

By taking the ratio of the noise power at two different sampling rates f_{p1} and f_{p2}, the factor Δf^2 is eliminated such that:

$$G(f_{p1}, f_{p2}, a, b) = \frac{W_{ab}(f_{p1})}{W_{ab}(f_{p2})} \qquad (3\text{-}12)$$

Where: G is some function. It is believed that this noise is due to quantization. The following analysis corroborated this contention.

In chapter one it was stated that the performance of a delta modulator, in normal operating condition, is affected by a noise which originates from the quantization process. Recalling equation 1-17, which gives signal-to-quantization ratio and rewriting this equation here for convenience:

$$S^2/N_q^2 = \frac{1}{8\pi^2 K_q} \cdot \frac{f_p^3}{f_c f_s^2} \qquad (3\text{-}13)$$

Where: K_q is a constant and approximately equal to 1/3,

S^2 is input signal power,

f_s is the frequency of the input signal,

f_c is the cutoff frequency of an output low-pass filter, i.e. the system bandwidth.

For a certain amplitude E_s and frequency f_s of a sinusoidal input signal, provided that the system stays in its normal operating condition, the quantization noise power N_q^2, can be written as:

$$N_q^2 = K f_c \frac{1}{f_p^3} \qquad (3\text{-}14)$$

Where: $K = 8\pi^2 K_q S^2 f_s^2$ and depends on the input signal condition.

The above analysis shows that, for a given bandwidth f_c, and by sampling a constant input signal at different sampling rates f_p, the product $N_q^2 f_p^3$ is a constant, or the ratio of the quantization noise at any two sampling rates f_{p1} and f_{p2} is:

$$\frac{N_{q1}^2}{N_{q2}^2} = \left(\frac{f_{p2}}{f_{p1}}\right)^3 \qquad (3\text{-}15)$$

Therefore, if the noise shown in figures 3-17 - 3-19 is due to quantization, then equations 3-12 and 3-15 should be representable by:

$$G = \left(\frac{f_{p2}}{f_{p1}}\right)^3 \qquad (3\text{-}16)$$

This was corroborated by computing the noise power at each sampling rates, (appendix-2) following the approach used in deriving equation 3-12; i.e. straight line approximation of the noise spectrum envelope shown in figure 3-17 - 3-19. The difference between the computed value of G and the theoretically expected ratio $(f_{p(n+1)}/f_{pn})^3$ in table 3-2 is due to the straight line approximation of the noise spectrum distribution.

As the locally decoded waveform is a stepwise waveform, its envelope contains overtone components in addition to the analogue information. These overtone components constitute both upper and lower side bands, centered at the sampling rate and its multiples.

F_c KHZ	Graphically computed noise power			G_{12}	F_{21}	% difference	G_{13}	F_{31}	% difference	G_{23}	F_{32}	% difference
	$W_{ab(f_{p1})}$	$W_{ab(f_{p2})}$	$W_{ab(f_{p3})}$									
0.5 - 3.0	5.45	0.455	0.0625	11.98	8	49.7	87.2	64	36.25	7.28	8	-9.0
0.5 - 4.0	7.08	1.031	0.120	6.87	8	-14.16	59	64	-7.8	3.59	8	7.4
0.5 - 5.0	7.98	1.61	0.220	4.96	8	33.0	36.27	64	-43.3	7.32	8	-8.5
2.0 - 5.0	5.70	1.46	0.183	3.90	8	51.2	31.15	64	-51.3	7.98	8	2.0
Average ratios				7.02	8	-13	58.53	64	-12	8.71	8	+8.9

f_{p1} = 8.0 KHZ

f_{p2} = 16.0 KHZ

f_{p3} = 32.0 KHZ

$$G_{12} = \frac{W_{ab(f_{p1})}}{W_{ab(f_{p2})}} \qquad F_{21} = \left(\frac{f_{p2}}{f_{p1}}\right)^3$$

$$G_{13} = \frac{W_{ab(f_{p1})}}{W_{ab(f_{p3})}} \qquad F_{31} = \left(\frac{f_{p3}}{f_{p1}}\right)^3$$

$$G_{23} = \frac{W_{ab(f_{p2})}}{W_{ab(f_{p3})}} \qquad F_{32} = \left(\frac{f_{p3}}{f_{p2}}\right)^3$$

Table 3-2 - Comparison of the graphically computed noise power ratio G with the theoretically expected ratio F.

The general spectrum of such stepwise waveform is shown in figure 3-22. Mathematically, the presence of these overtone components is interpreted by the product of the Fourier series expansion of a periodic waveform at f_s with that of a train of a positive pulses at f_p. The Fourier series expansion of a periodic wave, is in the form of:

$$f_1(t) = \sum_{n=1}^{\infty} C_n \sin nw_s t \qquad (3\text{-}17)$$

That of the positive pulses is in the form of:

$$f_2(t) = \frac{a_o}{2} + \sum_{n=1}^{\infty} C_m \operatorname{Cos} mw_p t \qquad (3\text{-}18)$$

Therefore, the product of these two expansions yields to:

$$f_1(t).f_2(t) = \sum_{n=1}^{\infty} \frac{a_o C_n}{2} \sin nw_s t + \frac{C_n C_m}{2} \{\sin(mw_p - nw_s)t - \sin(mw_p + nw_s)t\} \qquad (3\text{-}19)$$

At each value of m, n assumes values of 1,2,... Furthermore, at m=o, the fundamental of $f_1(t)$ and its harmonics exists. At m=1 or higher, upper and lower side-bands are present. In the normal condition and for a sinusoidal input, the stepwise waveform follows a sinusoidal shape, whose frequency spectrum has only the fundamental. Therefore, at each value of m, n can have only the value of one. This is illustrated in figure 3-22. The amplitudes and the frequencies of the most predominent peaks are given in table 3-3. By passing the locally decoded wave through a low-pass filter, the quantization noise shown in figure 3-17 can be attenuated to some extent; whereas the overtone peaks and their accompanied noise occuring at high frequencies are attenuated to a negligible amount.

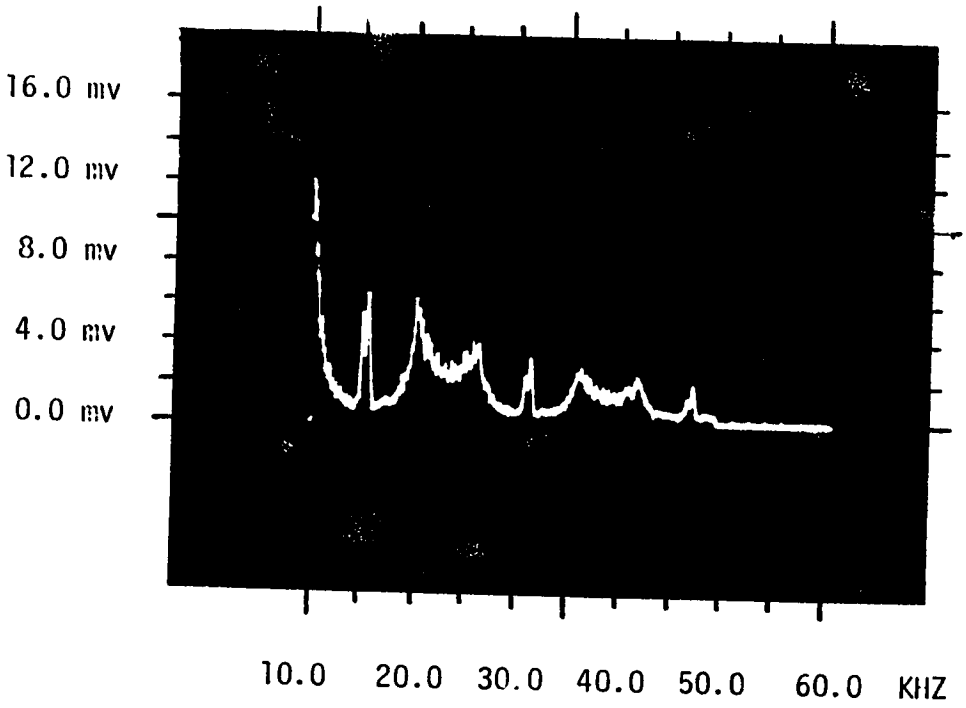


Fig. 3- 22- Frequency spectrum of the locally decoded waveform showing the overtone components at sampling rate and its multiples.

Overtone component	Amplitude mv	Frequency KHZ	Relative amplitude w.r.t. the fundamental
1st	6.0	16.0 $\pm$ 0.25	1.2 %
2nd	3.5	32.0 $\pm$ 0.25	0.7 %
3rd	2.0	48.0 $\pm$ 0.25	0.4 %

Fundamental amplitude = 500 mv at 250 HZ

Table 3-3 - Amplitudes of the overtone components at normal operating condition.

3-4.3 Slope overloading condition

The analogue input signal x(t) may be such that either its level E_s or its frequency f_s cause inequality 3-8 to be violated. Under such circumstances, the delta modulator is said to be a"slope overloaded" and the feedback signal y(t) is incapable of following the input. Figure 3-23 shows a condition where the system is slope overloaded. The digital output in this case is a sequence of consecu tive one's and then zero's. The repetition rate of these sequences

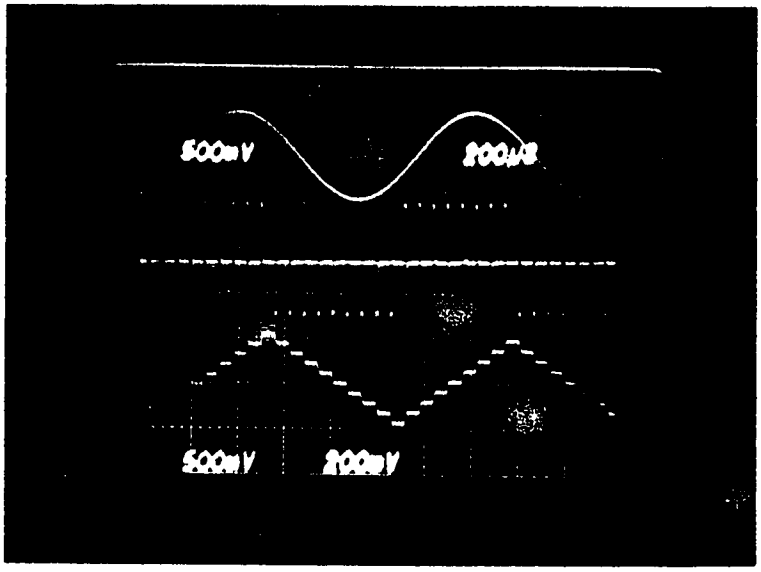


Fig. 3-23 - Linear delta modulator waveforms at slope overloading condition.

of consecutive values is same as that of the input signal f_s. Integration of this digital pattern leads to a stepwise triangular waveform again at a frequency equal to that of the input signal, but shifted by an angle ϕ. Theoretical analysis |4| shows that, this phase angle ϕ is at its maximum value ($\phi_{max}=32.5^o$), when equation 1-10 is satisfied. Figure 3-24 illustrates this phenomena and shows the reconstructed wave shifted by an angle $\phi=30^o$. This phase angle is lower than its maximum value because the condition satisfying equation 1-10 not yet reached.

A Fourier series expansion shows that the frequency spectrum of a triangular wave contains only the fundamental and its odd harmonics. The amplitudes and frequencies are given by |18|:

$$f(w_t) = \frac{8}{\pi} \sum_{n=odd} \frac{1}{n^2} \text{Sin } nwt \qquad (3\text{-}20)$$

Where: $w = 2\pi f$ is the fundamental frequency of the triangular waveform. This was corroborated by the frequency spectrum analysis of the stepwise triangular waveform (Figures 3-25 and 3-26). Overtone components of the fundamental and its odd harmonics consisting both upper and lower side-bands having the sampling rate f_p and its multiples as the carrier are shown in figure 3-27. The interpretation of these components is same as that at that given for figure 3-22. The periodic wave at the output of the decoder in this case, has a triangular shape. Here at each value of m, n can have its odd

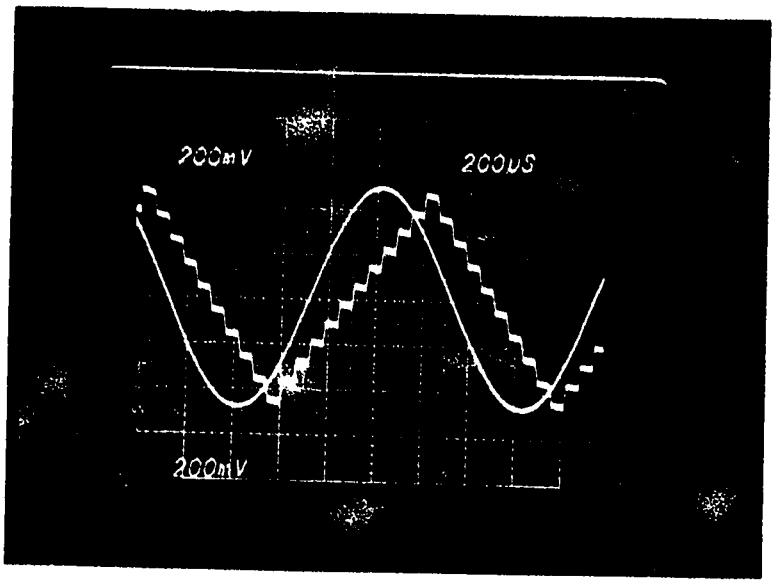


Fig. 3-24 - Sinusoidal input and its stepwise approximation shifted by an angle ϕ.

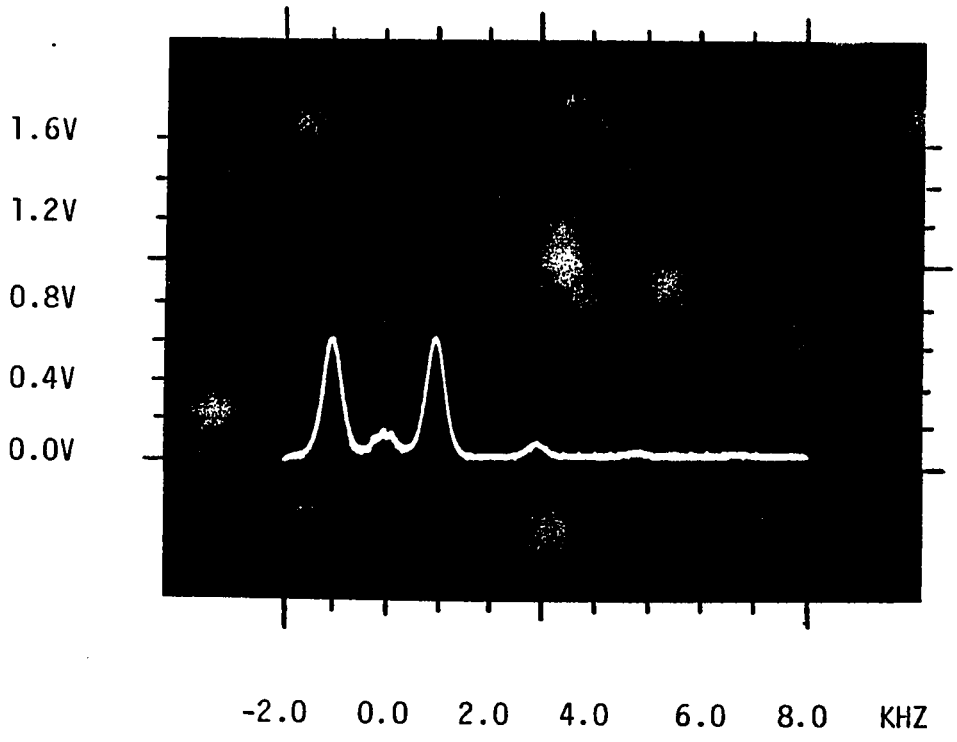


Fig. 3-25 - Reconstructed triangular waveform as displayed by the spectrum analyzer.

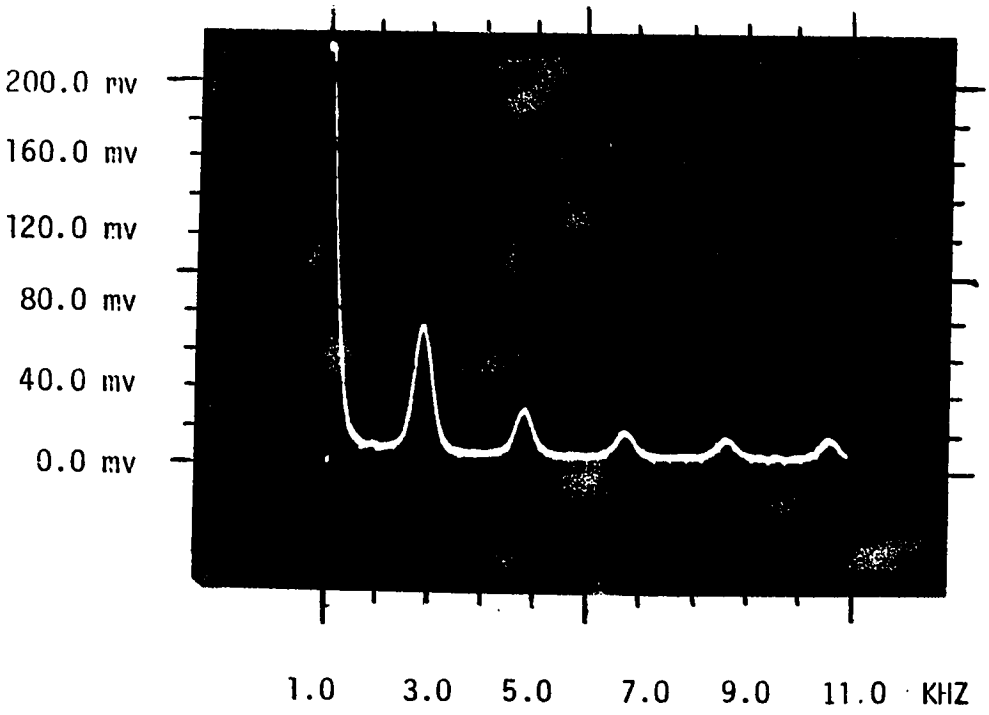


Fig. 3-25 - Spectrum analyzer display showing the odd harmonics of the reconstructed triangular waveform.

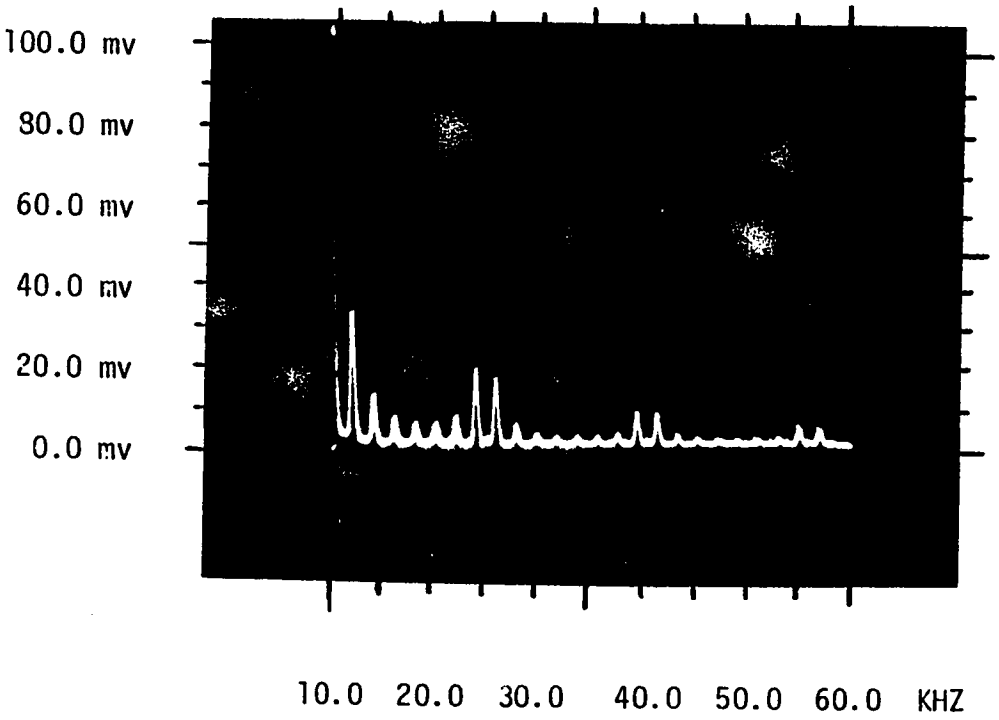


Fig. 3-27 Frequency spectrum of the reconstructed triangular wave over a 1-60 KHZ showing the overtones and their harmonics.

numbers. The theoretically computed and the measured peaks of the fundamental and its odd harmonics together with their corresponding frequencies are listed in table 3-4. The percentage differences between the measured and computed peaks ranges from 4% to 25%. The error is greater at higher harmonics, since these harmonics are superimposed by the lower sideband harmonics of the first overtone component occuring at same frequencies. Table 3-5 shows the amplitudes and the frequencies of the overtone components together with their relative amplitudes with respect to the fundamental.

Because of low frequency components, even by passing the decoded triangular wave through a low-pass filter, there may still be appreciable harmonic distortion. The result may be a considerable amount of noise, exceeding that of quantization noise. The peaks of the components occuring at sampling rate and its multiple generally do not cause major problems, since a low-pass filter can appreciably attenuates them.

3-4.4 Frequency response

The frequency response characteristic of a LDM system can be predicted theoretically, using the slope overloading property. It was stated before that, at grossly slope overloading condition, the digital pattern at the output of the encoder is a sequence of consecutive one's and zero's. The quantity of these one's and zero's in one cycle is controlled by the ratio of sampling rate f_p to the frequency of the input signal f_s. The integration of these digital

n	Measured values		Computed amplitude mv	% difference
	Amplitude mv	Frequency KHZ		
Fundamental (n = 1)	400.0	1.0	385.0	3.9
3	44.0	3.0	43.0	2.5
5	17.0	5.0	15.4	10.4
7	10.0	7.0	8.0	25.0

Table 3-4 - Measured and computed amplitudes of the decoded stepwise triangular wave.

Overtone component	Amplitude mv	Frequency KHZ	Relative amplitude w.r.t. the fundamental
1st	25.0	16.0 $\pm$ 1.0	6.25 %
2nd	10.0	32.0 $\pm$ 1.0	2.50 %
3rd	6.0	48.0 $\pm$ 1.0	1.50 %

Fundamental amplitude = 400 mv at 1000 HZ

Table 3-5 - Amplitudes of the overtone components at slope overloading condition.

values, assuming positive and negative impulses, is a stepwise triangular wave. The frequency of a sinusoidal input at which the system is completely slope overloaded can be calculated using the condition given by equation 1-10; i.e.:

$$f_s^* = 1.86 \frac{\Delta . f_p}{2\pi E_s} \qquad (3\text{-}21)$$

Equation 3-21 is applicable for a sinusoidal input having an amplitude E_s. Different input amplitudes result in different values for f_s^*. At f_s^* or above the number of consecutive one's and zero's in one cycle is given by:

$$\text{No. of one's + No. of zero's} = \frac{f_p}{f_s^*} \qquad (3\text{-}22)$$

and for a symmetrical triangular waveform:

$$\text{No. of one's} = \text{No. of zero's} = \frac{f_p}{2f_s^*} \qquad (3\text{-}23)$$

At each consecutive one or zero the feedback signal y(t) changes by Δ volts, therefore the peak-to-peak amplitude of the stepwise triangular wave at f_s equal to f_s^* is given by:

$$y^*(t) = \frac{f_p}{2f_s^*} \cdot \Delta \qquad (3\text{-}24)$$

which can be expressed in DB as:

$$y^*(t)_{DB} = 20 \log\left(\frac{f_p}{2f_s^*} . \Delta\right) \qquad (3\text{-}25)$$

For any value of f_s greater than f_s^*, equation 3-25 can be rewritten as:

$$y(t) = 20 \log \frac{f_p \cdot \Delta}{2} \quad 20 \log f_s \qquad (3\text{-}26)$$

At a constant sampling rate f_p, and a fixed step size Δ, equation 3-26 represents a straight line with an assymptotic break point at f_s^*. The rate at which $y(t)$ varies with f_s is determined as follow:

Considering two frequencies f_{s1} and f_{s2} such that $f_{s2} > f_{s1}$, the amplitudes of $y_1(t)$ and $y_2(t)$ are:

$$y_1(t) = 20 \log \frac{f_p \cdot \Delta}{2} - 20 \log f_{s1}$$

$$y_2(t) = 20 \log \frac{f_p \cdot \Delta}{2} - 20 \log f_{s2}$$

Then:

$$y_1(t) - y_2(t) = - 20 \log f_{s1} + 20 \log f_{s2} = 20 \log \frac{f_{s2}}{f_{s_1}} \qquad (3\text{-}27)$$

If $f_{s2} = 10\ f_{s1}$, then the change in $y(t)$ is 20 DB. This shows that the amplitude of the feedback signal $y(t)$ at f_s greater than f_s^*, rolls off at a rate of 20 DB/decade.

In order to predict the frequency response of a LDM system, the following steps are required to follow:

1) Choose an input level E_s e.g. 0.0 dB,
2) Calculate f_s^* using equation 3-21,
3) Calculate $y(t)^*$ using equation 3-24

Choosing different amplitudes of the input signal, different bandwidths are obtained. The method is applicable only with a sinusoidal signal as an input for assymptotic results. Rounding, where the system starts to be slope overloaded, is difficult to consider theoretically due to irregularity of the digital pattern at the output of the encoder. The graphical transfer function characteristic of the implemented delta modulator was calculated and is shown in fig. 3-28. A sampling rate of 16 KHZ and a step size of 120 mv are incorporated within the calculations. The calculated values of f_s^* at different input levels and their corresponding amplitudes of $y(t)^*$ are tabulated in table 3-6. The fundamental of the triangular wave was used as the output signal, in plotting the curves.

Figure 3-29, shows the transfer function characteristic using the data obtained by running a frequency response test. The amplitudes of the reconstructed wave at different frequencies were read on the spectrum analyzer (table 3-7). The fundamental of the triangular output was used as an output signal during the slope overloading regions. The flat region in the theoretical curves was not calculated, but since it represents the tracking region, the system was assumed to have a unit gain; i.e. the output after filtering is equal to the input. The measured curves supports the validity of this assumption. The theoretically expected bandwidths and the measured one's, at different input amplitudes are

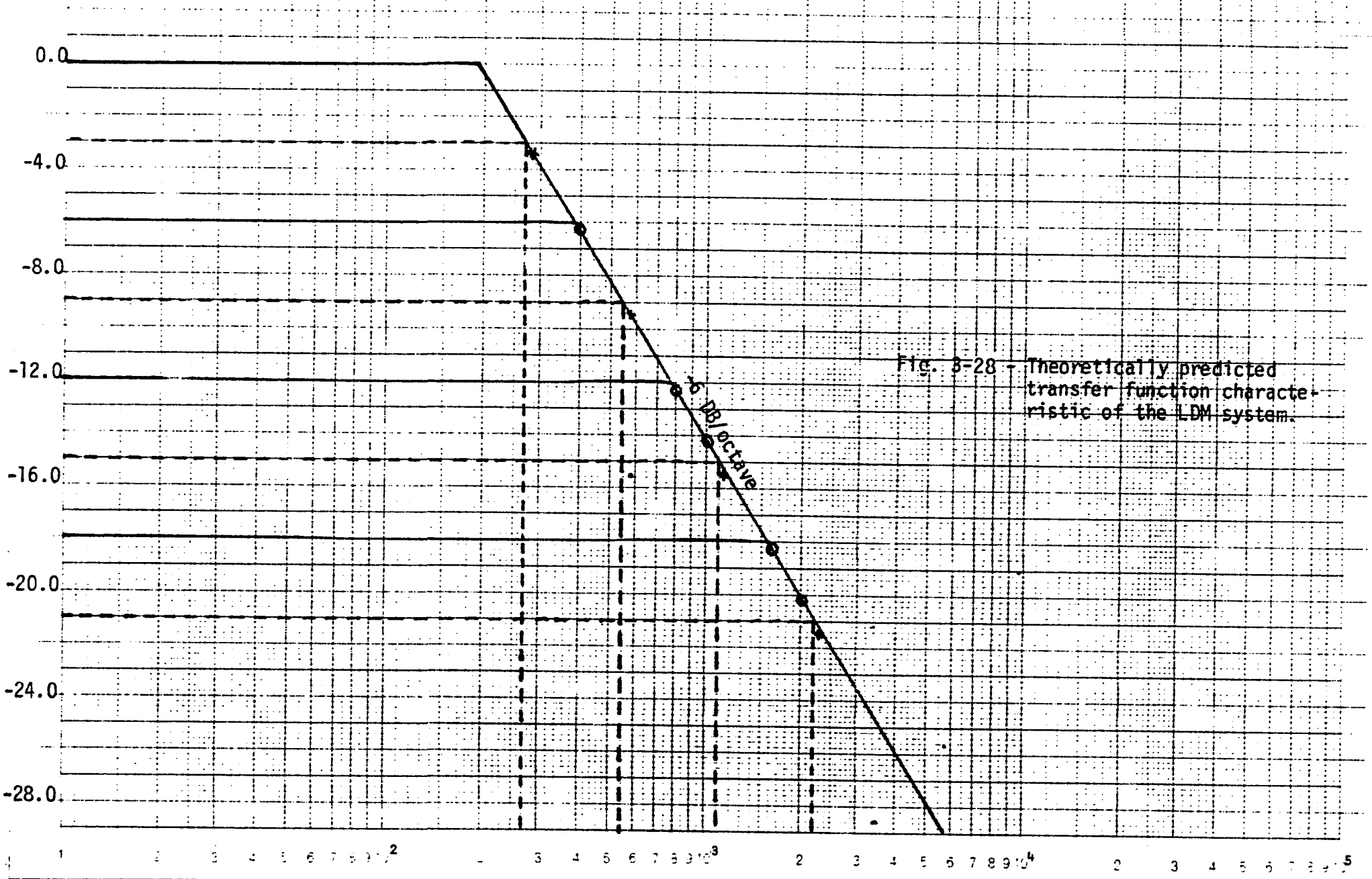


Fig. 3-28 - Theoretically predicted transfer function characteristic of the LDM system.

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Input level = E_s		$f_s^* = \frac{1.86\ \Delta f_p}{2\pi E_s}$ HZ	No. of "1"s or "0"s = $f_p/2f_s$ f_p = 16 KHZ	Triangular output; i.e. y(t). V_{P-P}	Fundamental of y(t). V_{P-P}	V_o/V_i DB
V_{P-P}	DB					
4.0	0.0	284	28	3.36	2.72	-3.35
2.0	-6.0	568	14	1.68	1.36	-9.35
1.0	-12.0	1136	7	0.84	0.68	-15.35
0.5	-18.0	2272	4	0.42	0.34	-21.35

Table 3-6 - Cutoff frequency f_s^* at different input levels and corresponding stepwise triangular reconstructed wave y(t).

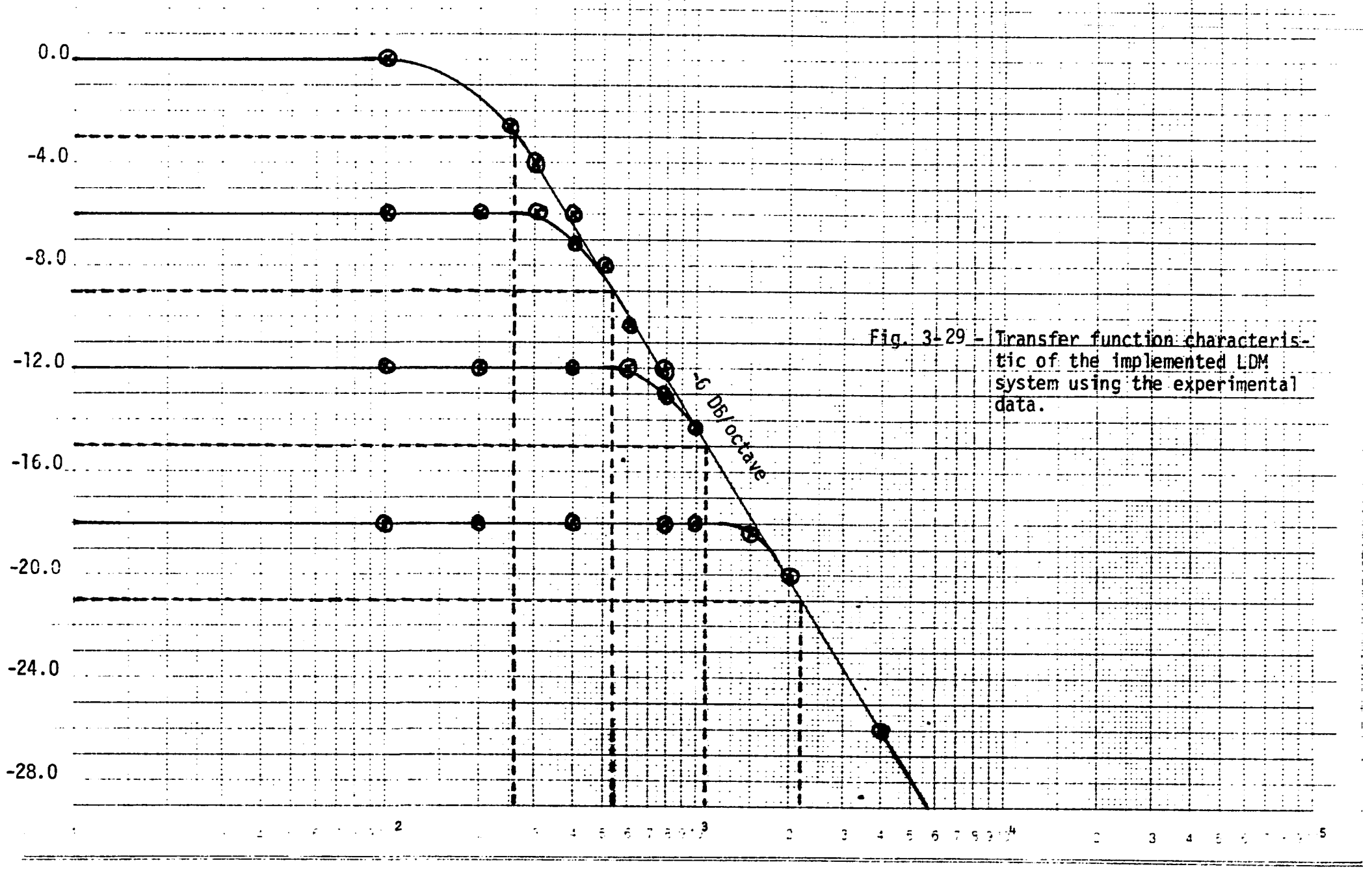


Fig. 3-29 - Transfer function characteristic of the implemented LDM system using the experimental data.

Input cond. peak value	2.0 V 0.0 DB		1.0 V -6.0 DB		0.5 V -12.0 DB		0.25 V -18.0 DB	
Output peak value at f_S	Volt	DB	Volt	DB	Volt	DB	Volt	DB
100	2.0	0.0	1.0	-6.0	0.5	-12.0	0.25	-18.0
200	2.0	0.0	1.0	-6.0	0.5	-12.0	0.25	-18.0
250	1.48	-2.6	1.0	-6.0	-	-	-	-
300	1.26	-4.0	1.0	-6.0	-	-	-	-
400	1.00	-6.0	0.88	-7.1	0.5	-12.0	-	-
500	0.80	-8.0	0.70	-9.1	-	-	0.25	-18.0
600	0.68	-9.4	0.60	-10.4	0.5	-12.0	-	-
700	0.56	-11.1	0.50	-12.0	0.49	-12.2	-	-
800	0.50	-12.0	0.46	-12.7	0.45	-13.0	-	-
900	-	-	-	-	0.40	-14.0	-	-
1000	0.40	-14.0	0.37	-14.6	0.36	-14.8	0.25	-18.0
1200	0.34	-15.4	0.30	-16.5	0.3	-16.5	0.25	-18.0
1500	0.26	-18.4	0.24	-18.4	0.24	-18.4	0.24	-18.4
1800	-	-	-	-	-	-	-	-
2000	0.20	-20.0	0.20	-20.0	0.2	-20.0	0.2	-20.0
3000	0.12	-24.4	0.12	-24.4	0.12	-24.4	0.12	-24.4
4000	0.10	-26.0	0.1	-26.0	0.1	-26.0	0.1	-26.0

Table 3-7 - Experimental frequency response data.

given in table 3-8. The difference between the two bandwidths is quite small, however an error upto 4% probably results from reading spectrum analyzer's display. The approach described above is quite simple and one can estimate the performance of a LDM system in very short time.

Input condition (peak value)		Theoretical cutoff freq. HZ	Measured cutoff freq. HZ	% difference
V	dB			
2.0	0.0	270	260	4.0 %
1.0	-6.0	540	530	2.0 %
0.5	-12.0	1080	1070	1.0 %
0.25	-18.0	2160	2200	2.0 %

Table 3-8 - Theoretically expected and experimentally resulting bandwidthsfor the implemented LDM system.

CHAPTER - 4

COMPANDED DELTA MODULATION SYSTEMS

4-1. Introduction

This chapter describes the companding technique, which is a means to improve the performance of the delta modulator. Both instantaneous and syllabic companded delta modulators are included to show how companding improves the performance. Continuous variable slope delta (CVSD) modulators, built as integrated circuits chips by the Motorola and Harris semiconductors, are used as vehicles for the descriptions. These IC's provide simple design techniques to encode/decode speech signals, at relatively low sampling rates.

4-2. Companded DM Systems

The linear delta modulator suffers the disadvantage of a severely limited dynamic range for an acceptable signal to quantization noise ratio. A means of effectively increasing the dynamic range is "companding" (compressing-expanding) |4|. The general operation of companding is to compress large amplitude levels in the signal relative to smaller amplitudes prior to encoding. In this way the input level to the encoder can be maintained close to the value which gives the maximum signal-to-noise ratio. In the decoder an expanding process is used to compensate for the distortion in the input signal caused by compressing.

Most DM systems do not perform companding in the manner just described. Usually the derivative of the encoded signal is monitored to determine if the condition specified by equation 1-9 is satisfied and the step size is changed to prevent slope overload. That is, the system is self regulating or adaptive, so that optimum performance (maximum S/N) is achieved over a broad range of the input signal variation.

The companding schemes can be grouped into two categories; namely: "instantaneous" companding or "syllabic" companding. In the former, the step size is varied in discrete increments and depends on a function of discrete variables such as the history of the error signs. Whereas, in the latter technique, the change in the step size is a function of continuous variables such as the average power of the input signal over some time interval. Both syllabic and instantaneous companding have their own advantages. Syllabic companding has superior performance when speech is used and instantaneous companding is better where large changes in signal may occur such as for television communications.

4-3. Instantaneously Companded DM System

Instantaneously adaptive delta modulators incorporate discrete adaptation. The feedback signal to the error point may make significant changes, during a sampling instant r, in response to the polarity history of the output binary signal L(t). Successive bits L_r and L_{r-1} are compared to detect probable slope overload

(sign L_r=sign L_{r-1}) or probable granularity (sign $L_r \neq$ sign L_{r-1}). Such comparisons are used to determine the need to alter the step size. It is necessary to use logic decisions that in each instant can decide whether the step size should increase by a factor P or should decrease by a factor Q. The decision will be based on consecutive binary values. When they are all alike, the step size is increased, otherwise it is decreased. The simple bounds on the positive adaption parameters P and Q are: |19|

i) In order to adapt to the signal during slope overload, it is necessary that P is greater than one.

ii) In order to converge to a constant input signal during a purely "hunting" situation it is necessary that Q is smaller than one.

Using the above bounds on P and Q, the specified adaptation rule is given by |20|:

$$Y_r = P.Y_{r-1} \quad \text{if sign } L_r = \text{sign } L_{r-1} \qquad (4\text{-}1)$$

and

$$Y_r = Q.Y_{r-1} \quad \text{if sign } L_r \neq \text{sign } L_{r-1} \qquad (4\text{-}2)$$

Notice that if the adapting parameters P=Q=1, the system becomes the conventional linear delta modulation. Fig. 4-1 illustrates how slope overload and granularity tend to correspond, respectively, to occurance of like and unlike (successive) bits.

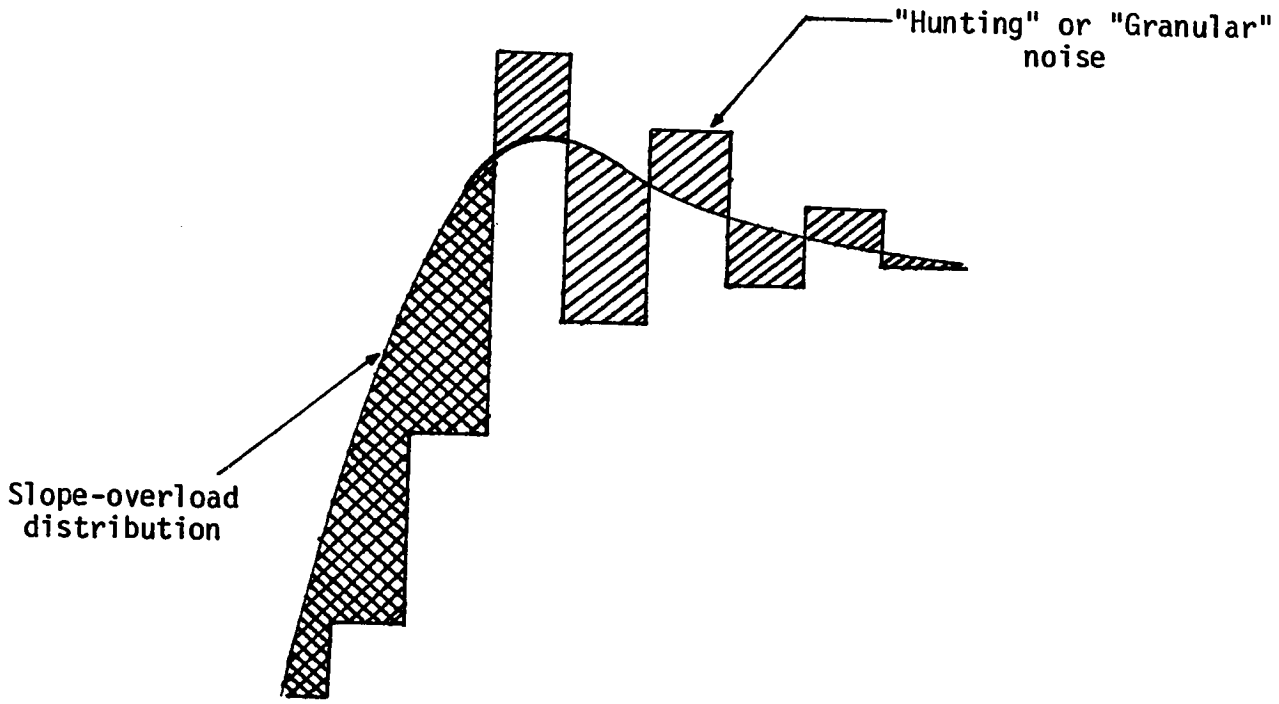


Fig. 4-1 - Illustration of adaptive delta modulation.

"High information delta modulation" (HIDM) invented by M.R. Winkler |1|, uses the values for P and Q, such that the step size is doubled whenever two identical consecutive binary levels appear i.e. P=2, and if the two consecutive binary levels are not identical in sign, the step size is lowered to half of its preceding value i.e. Q=0.5. It was shown by N.S. Jaynt |19| that in order to obtain optimum performance of an instantaneously adaptive delta modulation system, the optimal values for the adapting parameters are:

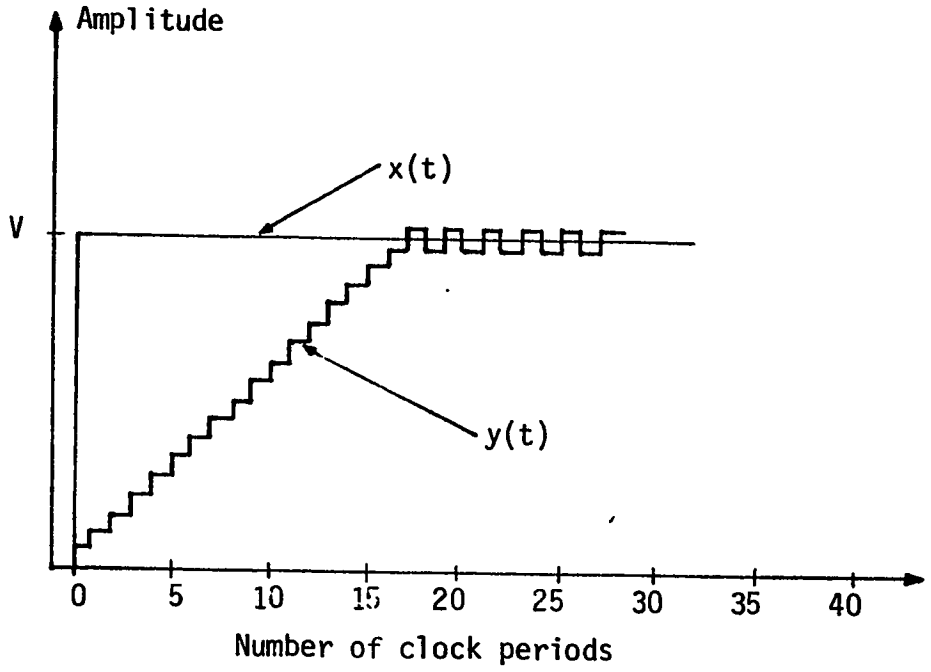
$$P_{opt} = 1.5$$

$$Q_{min} = 0.66$$

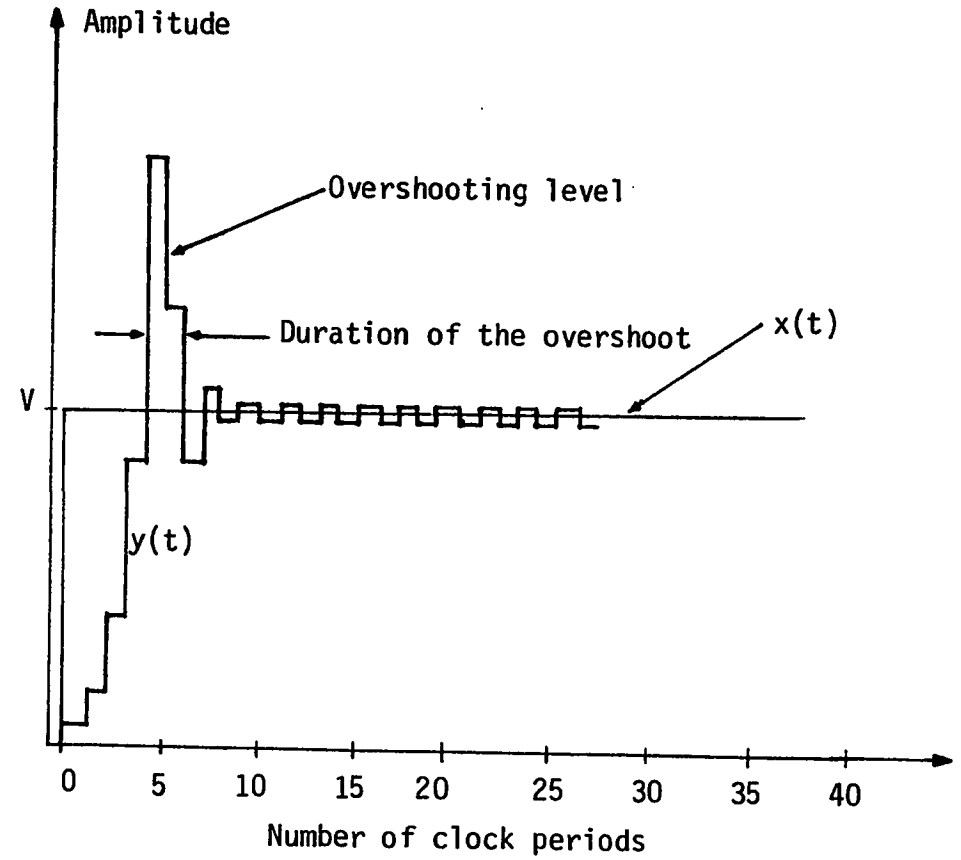
It was also shown that, for a stable system, it is necessary that:

$$P.Q \leq 1 \qquad (4\text{-}3)$$

The instantaneously companded DM can adapt its feedback signal y(t) to the input signal x(t) over a relatively small number of clock periods. This is illustrated in figure 4-2 for a step response. The figure illustrates how the instantaneously companded system, assuming P=2 and Q=0.5, hunts the constant amplitude input. Such companding yields much better fidelty than a LDM. The dynamic range is improved appreciably. Generally, the instantaneously companded system is accompanied with overshoot. The overshoot may have large amplitudes but very short time duration (see figure 4-2).



a) linear delta modulation system



b) Instantaneously companded system assuming P = 2 and Q = 0.5.

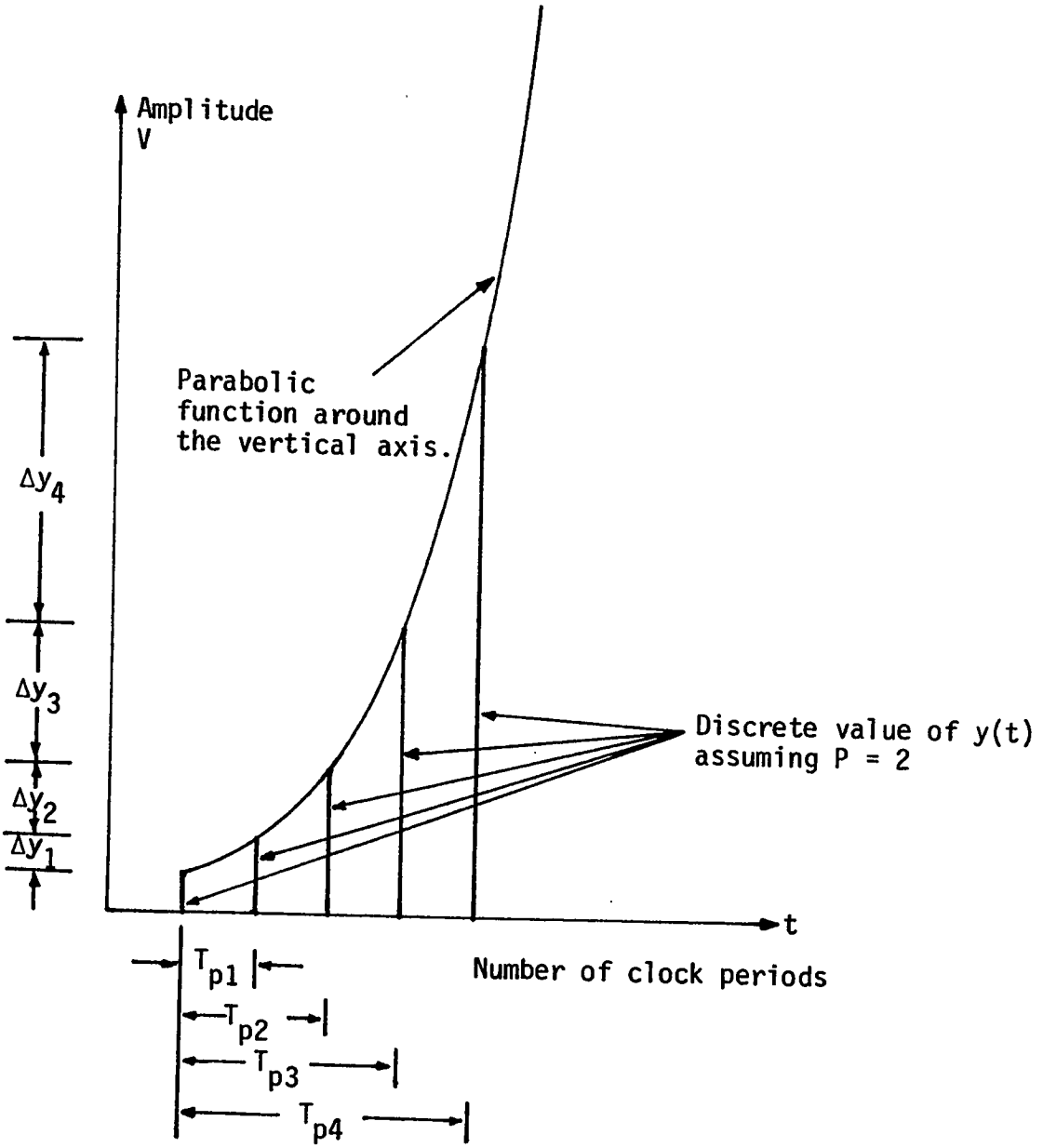
Fig. 4-2 - Step response of a LDM and of an instantaneously companded system.

This is because companding for a series of consecutive identical binary levels starts with a smaller step size and then grows by the factor P in discrete levels (usually, $1<P\leq 2$). This growth rate is shown in figure 4-3 and follows approximately a parabolic function around the vertical axis.

4-4. Syllabically companded DM system

Syllabically companded delta modulation systems, known also as "digitally controlled" or "continuous variable slope delta" (CVSD) modulation, reacts to the envelope rather than the instantaneous value of the input signal. The step size is determined (both at the transmitter and at the receiver) from the mean number of one's and zero's in the bit stream. Unlike the case of an instantaneous compander, the feedback step size y(t) is now adapted more smoothly in time, at a much slower rate |4|. This rate is, generally speaking, the pitch rate of the speech signal; i.e. in the order of 5-10 m sec (200 - 100 c/s) |4,5,11,21|.

Though the syllabic adaptation can be achieved by developing a control signal either from the analogue input, or from the digital output. A control signal derived directly from the analogue input is not suitable because it is not available at the receiver. Additionally, if the control signal is derived from the digital output of the encoder, tracking is more easily accomplished. Some delay is introduced between the transmitted and received signal which



$$\Delta y_4 = 2\Delta y_3,\ \Delta y_3 = 2\Delta y_2,\ \Delta y_2 = 2\Delta y_1$$

Fig. 4-3 - Step size variation for a series of consecutive identical binary levels in an instantaneously companded DM system.

corresponds to a phase difference between the two signals. However, the delay is not important in speech encoding |22|. The slow adaptation has the effect of decreasing granular noise at the cost of significant increase of slope overload distortion. The slope overload strategy ensures, a "clean sounding" at relatively low bit rates (below 25K bits/sec.) |21|. Continuous variable slope delta modulation system are mainly developed for handling a wider dynamic range of speech signals at a sampling frequencies of the order of 50 KHZ. These delta modulators also have a resistance to bit errors |21|.

Techniques, by different authors, implement CVSD system by using either analogue or digital functions in the feedback loop, to extract the analogue information from the digital bit stream. An analogue type of CVSD system is shown in fig. 4-4 where a low-pass filter F_e, a full wave rectifier, an envelope detector, and a multiplier are added in the feedback loop |4|. The digital pattern L(t) is passed through the filter F_e, having identical characteristics to the input filter F_i, it produces an analogue signal x(t) which is then full wave rectified, before being sent to the envelope detector (Figure 4-5). The envelope detector essentially behaves as a low-pass (syllabic) filter having a time constant approximating to the pitch rate of the speech signal; i.e. of the order of 10 ms. The output of the envelope detector $F_e(t)$ is multiplied with L(t) to produce the signal h(t). As L(t) is being multiplied by a signal which is always positive, it follows that h(t) has the

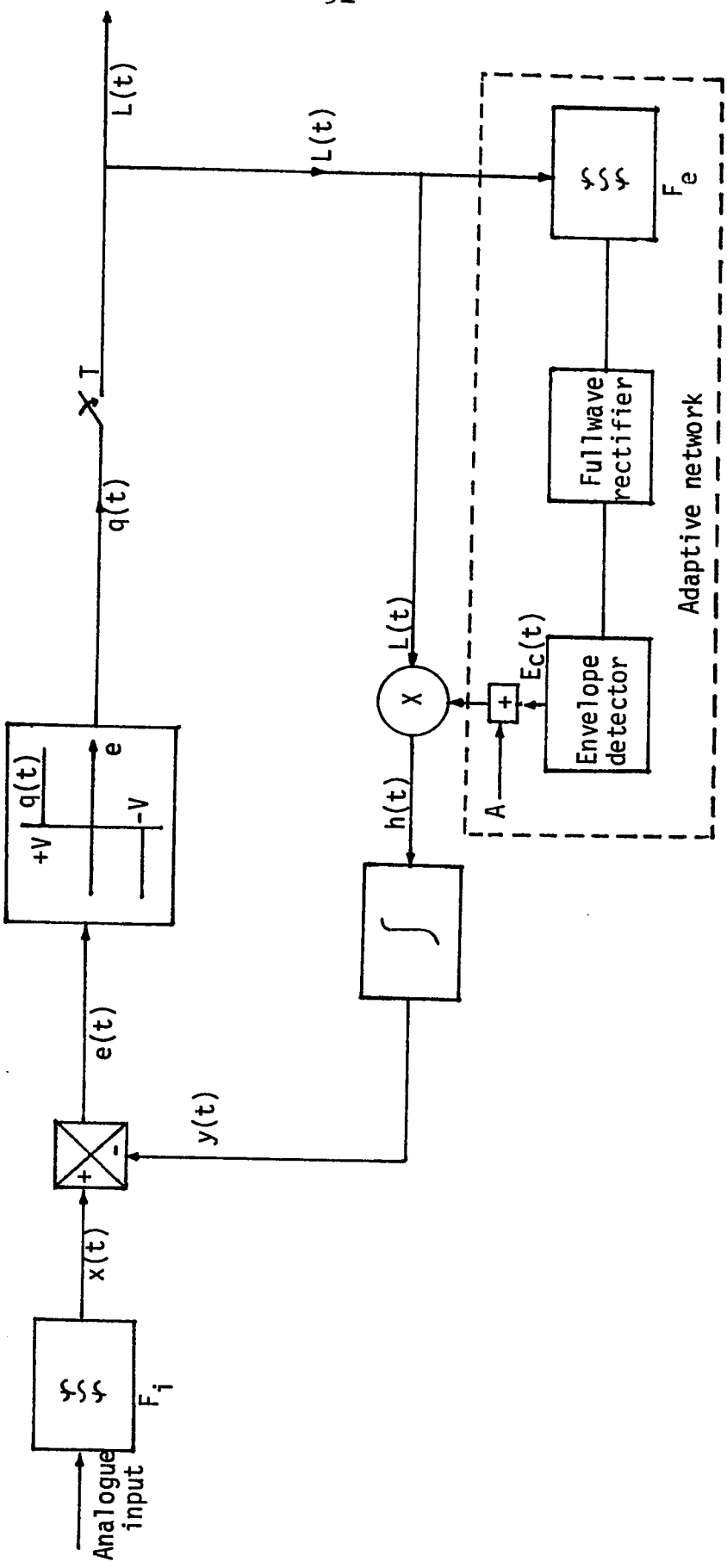
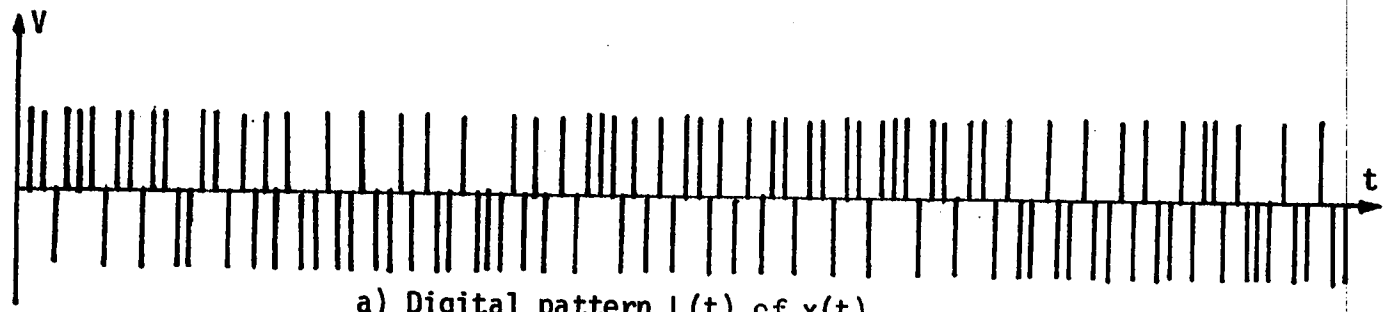
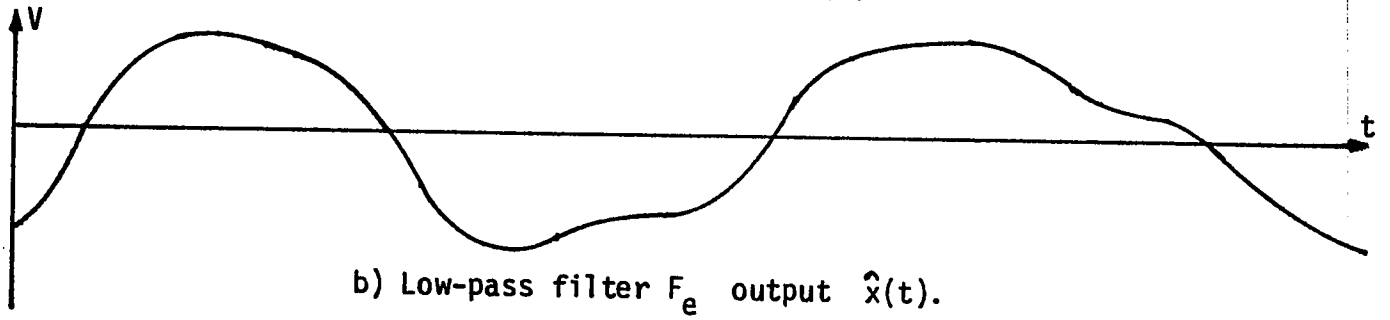


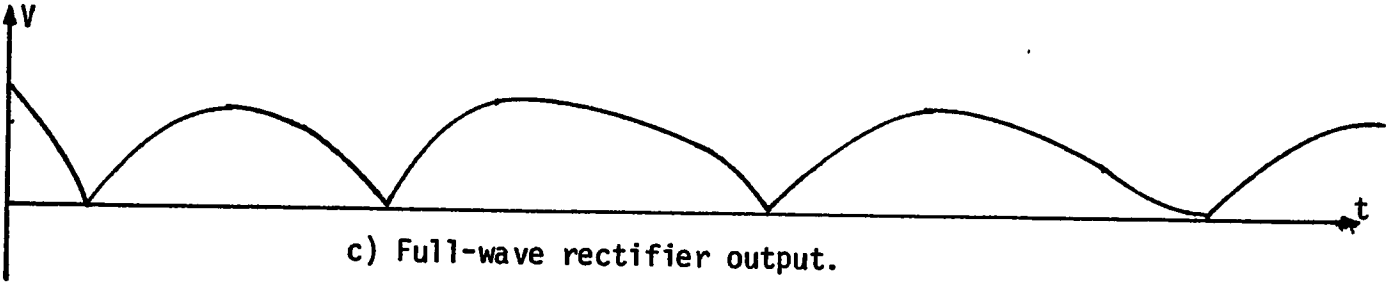
Fig. 4-4 - Analogue type of syllabically controlled delta modulator.



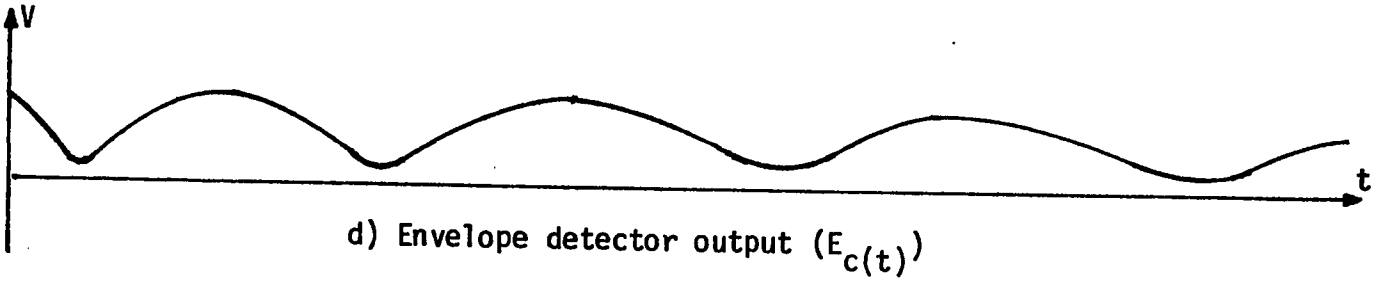
a) Digital pattern L(t) of x(t).



b) Low-pass filter F_e output $\hat{x}(t)$.



c) Full-wave rectifier output.



d) Envelope detector output ($E_{c(t)}$)

Fig. 4-5 - Intermediate waveforms to extract the syllabic control signal $E_{c(t)}$ from the digital pattern of an analogue signal x(t).

same polarity as those of L(t). Finally the h(t) signal is integrated to form y(t), enabling the encoder to vary the step amplitude according to the error pattern and the amplitude of the input signal x(t). At idling the L(t) pattern is a sequence of one's and zero's leading to a near zero output from the envelope detector. The y(t) signal in this condition changes by a minimum value, given by:

$$y(t)_{min} = \frac{1}{RC} \int_{0}^{T_p} AV \, dt + V(o) \qquad (4\text{-}4)$$

Where: RC is the time constant of the integrator,

V is the amplitude of the digital pattern L(t) and

A is a small d.c. signal added to the envelope detector output.

V(o) is the voltage on the capacitor at t=o

A CVSD system which uses a digital process for extracting the companding signal from L(t) is shown in Fig. 4-6. The additional digital logic acts as signal slope analyzer (SSA). The low-pass (syllabic) filter and a pulse amplitude modulator are also used. The companding action of this system is controlled by the algorithm designed into the signal slope analyzer (SSA), which measure, the slope of the incoming signal. This measure is implemented by looking for either a consecutive number of one's or zero's in a row. Generally 2 to 4 consecutive values are used to initiate companding. Therefore whenever this state exists at the output of the encoder, the SSA output is high (V_H) otherwise it is low (V_L). The output

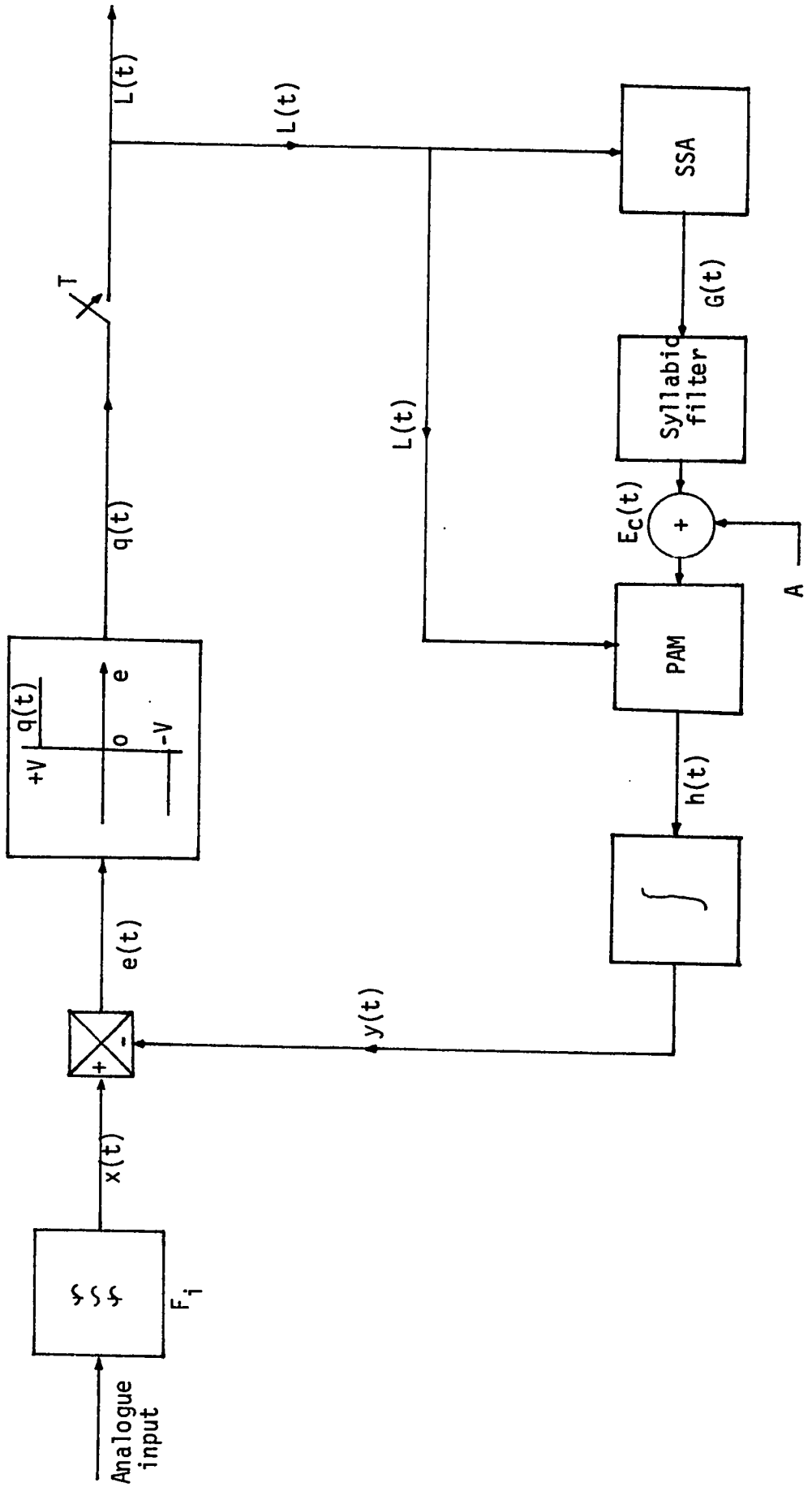


Fig. 4-6-Continuous variable slope delta modulator (CVSD).

of the SSA is passed through the syllabic filter and then to the (PAM) to yield a gradually changing value of the modulated step size. The polarity is preserved by the PAM output. The time constant of the syllabic filter is choosen to be in the range of 4-10 m sec because this value results in a good subjective performance when the speech signal is to be encoded |11| . The ratio of the maximum step size to the minimum step size, at the output of the integrator, is the companding improvement | 7,23 |. Under small input signals, when x(t) is insufficient to cause the logic output to go to its higher state, the encoder is uncompanded and behaves as a simple linear delta modulator. For this condition the step size is at its minimum value, given by equation 4-4.

A larger input signal, is characterized by consecutive strings of one's or zero's as the encoder attempts to track the input. The logic input to the syllabic filter actuates whenever n or more consecutive one's or zero's are present in the data. When this happens, the syllabic filter output starts to increase, thereby increasing the multiplier gain. Consequently the integrator output yields larger steps, enabling the system to track the more rapidly changing input. For very rapid input changes a condition will be reached where the system starts to be slope overloaded. At severe slope overloading,the waveforms at the output of the encoder and the output of the signal slope analyzer (SSA) are shown in fig. 4-7. The waveform G(t) at the output of the SSA can be expressed as:

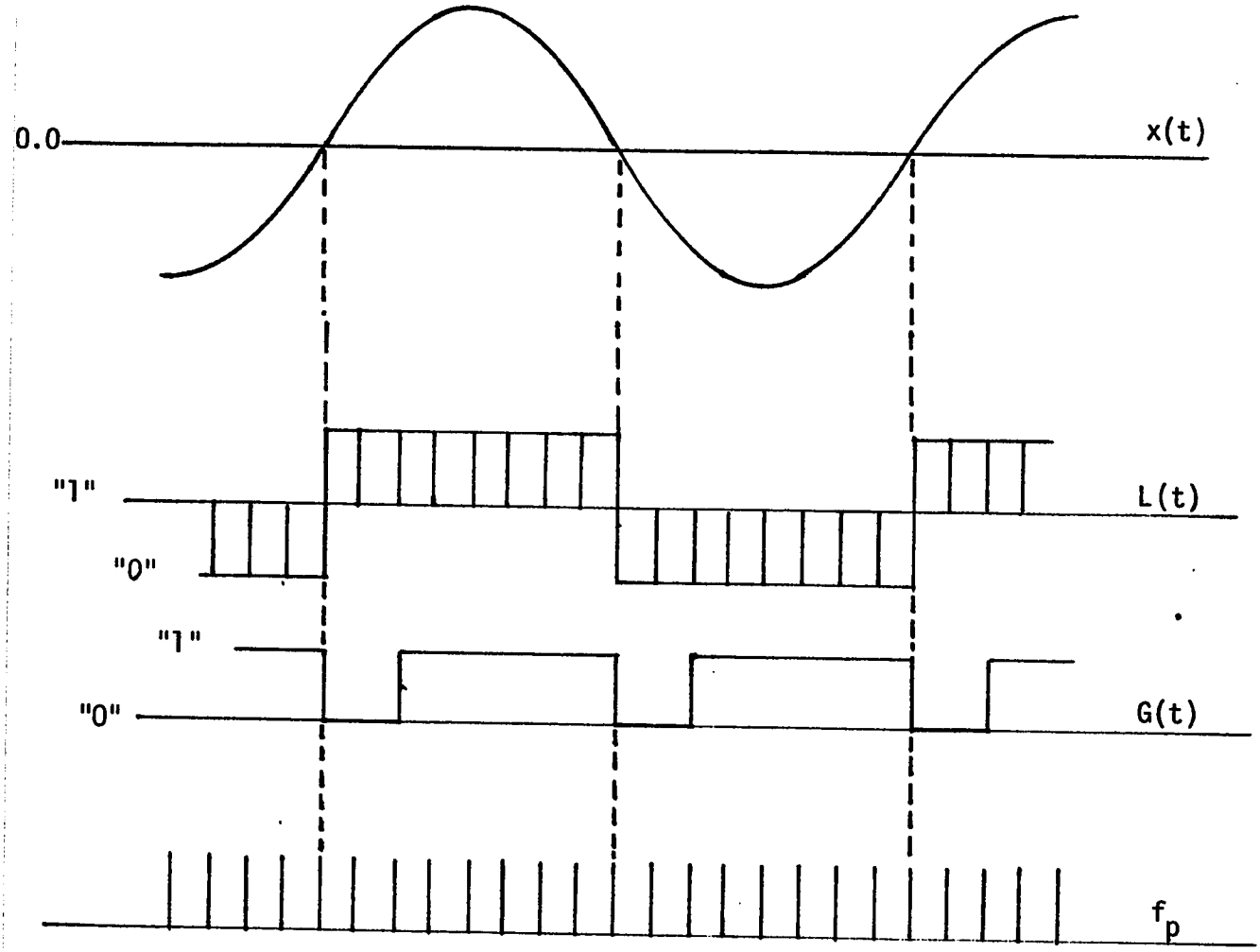


Fig. 4-7 - L(t) and G(t) waveforms for a sinusoidal input x(t) which grossly overloads the encoder at $f_p=16f_s$ and n=3.

$$G(t) = \begin{cases} V_L & \text{If the L(t) has no consecutive one's or zero's, or their numbers are less than (n)} \\ V_H & \text{If the L(t) contain at least (n) consecutive number of one's or zero's in a row.} \end{cases}$$

Where: n is the shift register length, (4-5)

V_H is the higher logic level representing the "1" state,

V_L is the lower logic level representing the "0" state.

Number of bits N, in L(t) waveform for one complete cycle of the input is given by the ratio of the sampling rate f_p to the input frequency f_s; i.e.

$$N = \frac{f_p}{f_s} \quad \text{bits} \tag{4-6}$$

A symmetrical encoder generates an equal number of one's and zero's in one cycle so that:

$$\text{No. of one's} = \text{No. of zero's} = \frac{N}{2} = \frac{f_p}{2f_s} \quad \text{bits} \tag{4-7}$$

The SSA output G(t), may be re-expressed for a time domain such as:

$$G(t) = \begin{cases} V_L & 0 \leq t \leq (n-1)/f_p \\ V_H & (n-1)/f_p \leq t \leq \left[\frac{f_p}{2f_s} - (n-1)\right]/f_p \end{cases} \tag{4-8}$$

The periodicity of the G(t) waveform is twice the input frequency f_s. For a single pole syllabic filter, its output rises exponentially. This output is known as "the control signal" $E_c(t)$, therefore:

$$E_c(t) = V_H(1-e^{-t/R_sC_s}) + E(0) \qquad (4-9)$$

Where: t is the time duration for which the SSA output will continue having the V_H state

$E(0)$ is the output of the filter at $t=0$

R_sC_s is the time constant of the syllabic filter.

At the slope overloading condition, the peak value of the adaptation control signal E_c is:

$$E_{c_{peak}}(t) = V_H\left[1 - e^{-\left[\frac{f_p}{2f_s} - (n-1)\right]/R_sC_sf_p}\right] + E(0) \qquad (4-10)$$

Equation 4-10 shows that if $\frac{f_p}{2f_s} = (n-1)$ i.e. the consecutive number of one's or zero's is equal to the shift register length n, the control signal $E_c(t)$ remains at $E(0)$ (usually $E(0)=0$). By definition, the logic output is at V_L state and the companding network does not function. The system at this ratio will generate the idling pattern; i.e. the minimum step size given by equation 4-4. For a given sampling rate, each value of shift register length n, has its corresponding value of f_s at which the adaptation network does not function. Table 4-1 gives these frequencies assuming different values of n at three different sampling rates.

n	$f_s = f_{p/2(n-1)}$		
	f_p = 16 KHZ	f_p = 32 KHZ	f_p = 64 KHZ
2	8.0 KHZ	16.0 KHZ	32.0 KHZ
3	4.0 KHZ	8.0 KHZ	16.0 KHZ
4	2.66 KHZ	5.33 KHZ	10.66 KHZ
5	2.0 KHZ	4.0 KHZ	8.0 KHZ
6	1.6 KHZ	3.2 KHZ	6.4 KHZ
7	1.33 KHZ	2.66 KHZ	5.33 KHZ
8	1.14 KHZ	2.29 KHZ	4.57 KHZ
9	1.0 KHZ	2.0 KHZ	4.0 KHZ

Table 4-1 - Bandwidths of the S.C.D.M. at three different sampling rates, assuming different values of shift register lengths (n).

The least value of n is 2, this is because if n is equal to 1, the shift register will act, as a delaying element and not as a signal slope analyzer. No algorithm could be found to select either the shift register length n or the syllabic filter time constant. Only some suitable values for speech encoding resulting from subjective choise are available |4,5,11,21|. But table 4-1 indicates that for a given sampling rate, the entire bandwidth of the system is determined by the value of n. Generally speaking, smaller values of n makes the companding network more responsive to changes in the input signal. This is because the output of the shift register algorithm actuates only when there is at least n number of identical binary levels at the output of the encoder. With low sampling rate such as 16 KHZ and for speech encoding the value of n should not be more than 3. This is because the system does not function beyond 4.0 KHZ for this value of n. At higher sampling rates such as 32 KHZ or 64 KHZ, it is advisable to use larger values of n to encode a speech signal over a much wider dynamic range. Table 4-1 shows that a total bandwidth of 4 KHZ is achievable, using n=3 at 16 KHZ, n=5 at 32 KHZ, and n=9 at 64 KHZ. In syllabically companded systems, the change in step size for a series of consecutive identical binary levels at the output of the encoder starts with a larger value and then diminishes gradually at the successive clock periods. This is because the syllabic filter voltage at the input of the multiplier is an exponential signal. The general form of the feedback signal y(t) is also

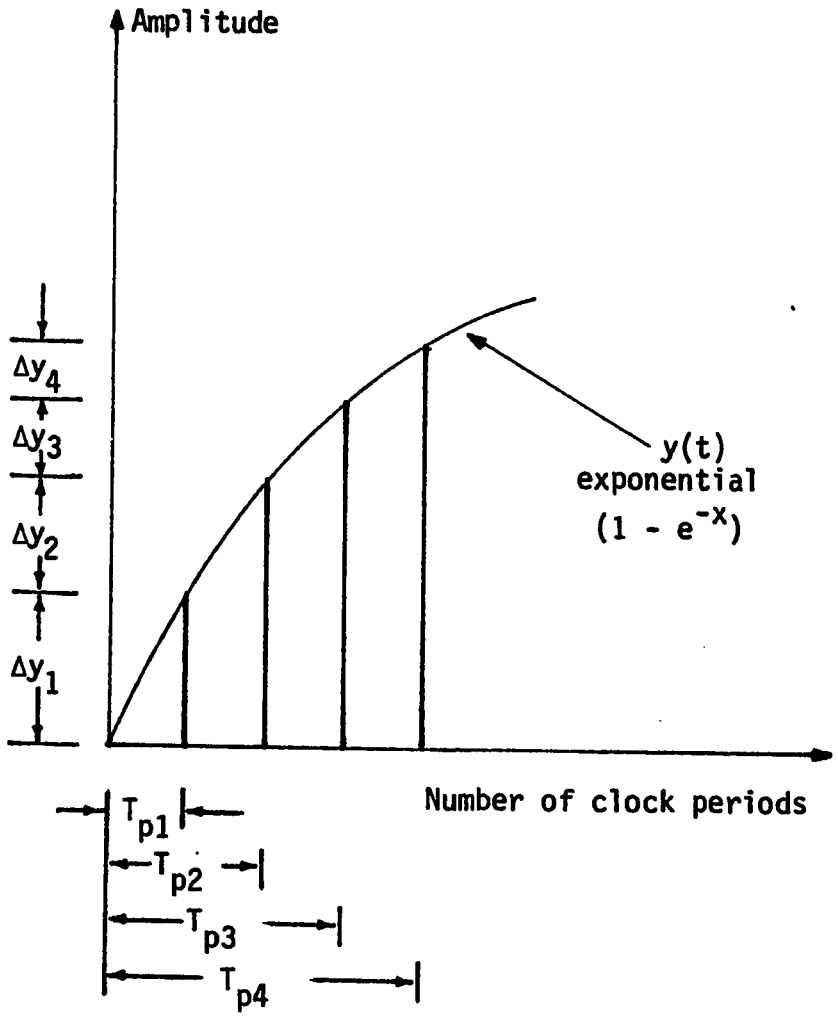
exponential. This type of signal has a low overshooting amplitude but may last for a long time. Figure 4-8 shows the step size variation in a syllabically companded delta modulation system.

4-5. Digital Integrated CVSD Modulators/Demodulators

Several manufacturers, such as Motorola, Harris and Consumer Microcircuits of America, have produced single-chip CVSD encoders that can also be used as decoders. For example the IC CVSD modulators (MC3417/MC3418), marketed by Motorola Semiconductors, contains all necessary active analogue and digital circuitry. The Harris semiconductor device (HC-55516/HC-55531) is nearly completely digital, including a digital filter. Digital summators (integrators) and digital multipliers drive a digital-to-analogue converter. The user of these chips needs only to apply the proper clock signal and the supply d.c. voltage. Few external resistors and capacitors are connected to suit the application. The use of large scale integration to produce delta modulators chips costing as little as $15.0 are opening new areas of application. The devices are even versatile enough for a host of non-telecommunications applications; e.g. programmable digital filters, remote controls, speech scrambling, and in instrumentation.

4-5.1 CVSD modulators by Motorola Semiconductors Co.

The Motorola Semiconductors Company designed and manufactured a series of integrated circuit chips of continuous variable slope delta modulators utilizing I^2L-linear bipolar technology |24,25|. These

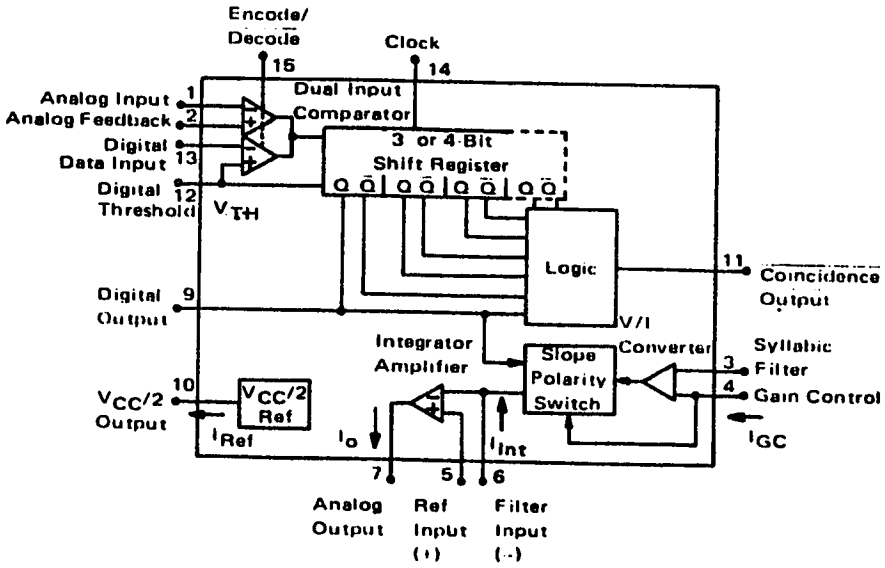


$$\Delta y_1 > \Delta y_2 > \Delta y_3 > \Delta y_4$$

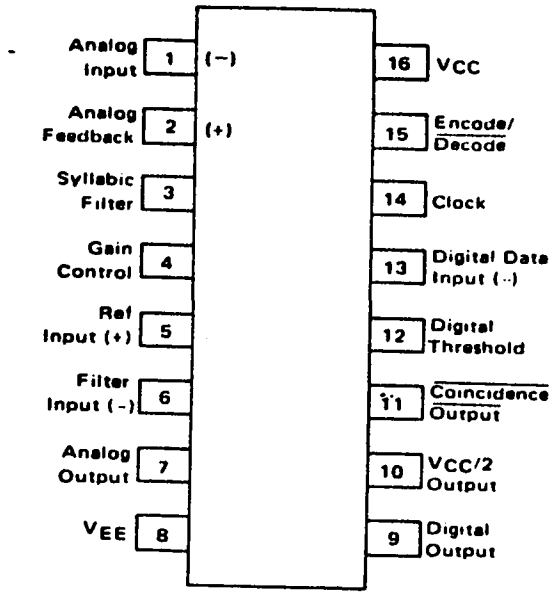
Fig. 4-8 - Step size variation for a series of consecutive identical binary levels in a syllabically companded DM system.

chips are characterized by CMOS compatible digital outputs and provide a simplified approach to digital speech encoding and decoding. A single IC may provide either encoding or decoding functions with a digital input for selection. The Motorola IC's are available in 16 pin flat packages with a 3-bit shift register algorithm (MC3417/MC3517) or with a 4-bit shift register algorithm (MC3418/MC3518) and in two temperature ranges. The MC 34XX series are useful for a temperature range from $0^{o}C$ to + $70^{o}C$ whereas the MC 35XX series are good for the range from $-55^{o}C$ to + $125^{o}C$. The integrated chips with a 3-bit shift registers are applicable for general communication purposes and those having 4-bit shift registers are good for telephone quality signals. A functional diagram and a pin layout are shown in figure 4-9. The maximum ratings and the electrical characteristics of the MC series are given in appendix-3a.

In general, the operating principles of the Motorola device (MC3417/3418 or MC3517/3518) is the same as described in section 4-3. The analogue comparator in the Motorola device replaces the differential amplifier and the quantizer in figure 4-5. Sampling is done by a D-type flip flop. The feedback loop contains three or four stages of D-type flip flops together with other logic circuits to function as the signal slope analyzer. Waveforms at the output of the encoder "Digital-out" at pin 9 and the signal slope analyzer output "$\overline{\text{Coincidence}}$ output" at pin 11 for a sinusoidal input, are as shown in figure 4-6, except that the shift register length "n" here is either 3 for the MC3417/3517 or 4 for the MC3418/3518. Motorola devices in general



a) Functional block diagram



b) Pin layout

Fig. 4-9 - Motorola IC CVSD system.

require an external syllabic filter between pins 11 and 3. Typical time constant values of 6 msec to 50 msec are used in voice codecs |25|. The slope polarity switch in the Motorola device behaves as the pulse amplitude modulator in figure 4-5 to convert the syllabically controlled signal according to the polarity of the L(t) pattern. A suitable capacitor connected between pins 6 and 7 is also required to obtain integration by the internally provided operational amplifier. The driving impedances at pins 1 and 2 should be nearly equal to avoid disturbing the idle channel characteristics. This is because, the analogue comparator was designed for low hysteresis (typically less than 0.1 mv) and high gain (typically 70 dB) |25|. The device has a maximum input bias-current of 1.5 μA |25|. Using either MC3417 or MC3418, the performance of the system is determined by the sampling rate (f_p), minimum step (Δ_{min}) and the total loop gain of the codec. Usually, for an optimum performance, the sampling rate should be nearer to the value specified by the manufacturer; i.e. 16 KHZ for the MC3417 or 32 KHZ for the MC3418/MC3518. However, the performance of the system can be altered by changing the loop gain of the system and the step size (Δ_{min}) at idling.

A simple CVSD encoder using the MC3417 or the MC3418 is shown in figure 4-10 |25|. The syllabic filter is a single pole RC network with a time constant of 6 msec. Selecting a standard value for C_s; i.e. 0.33 μf, the corresponding value of R_s is 18KΩ. The syllabic filter voltage, V_s appears across C_s (Figure 4-10) and is

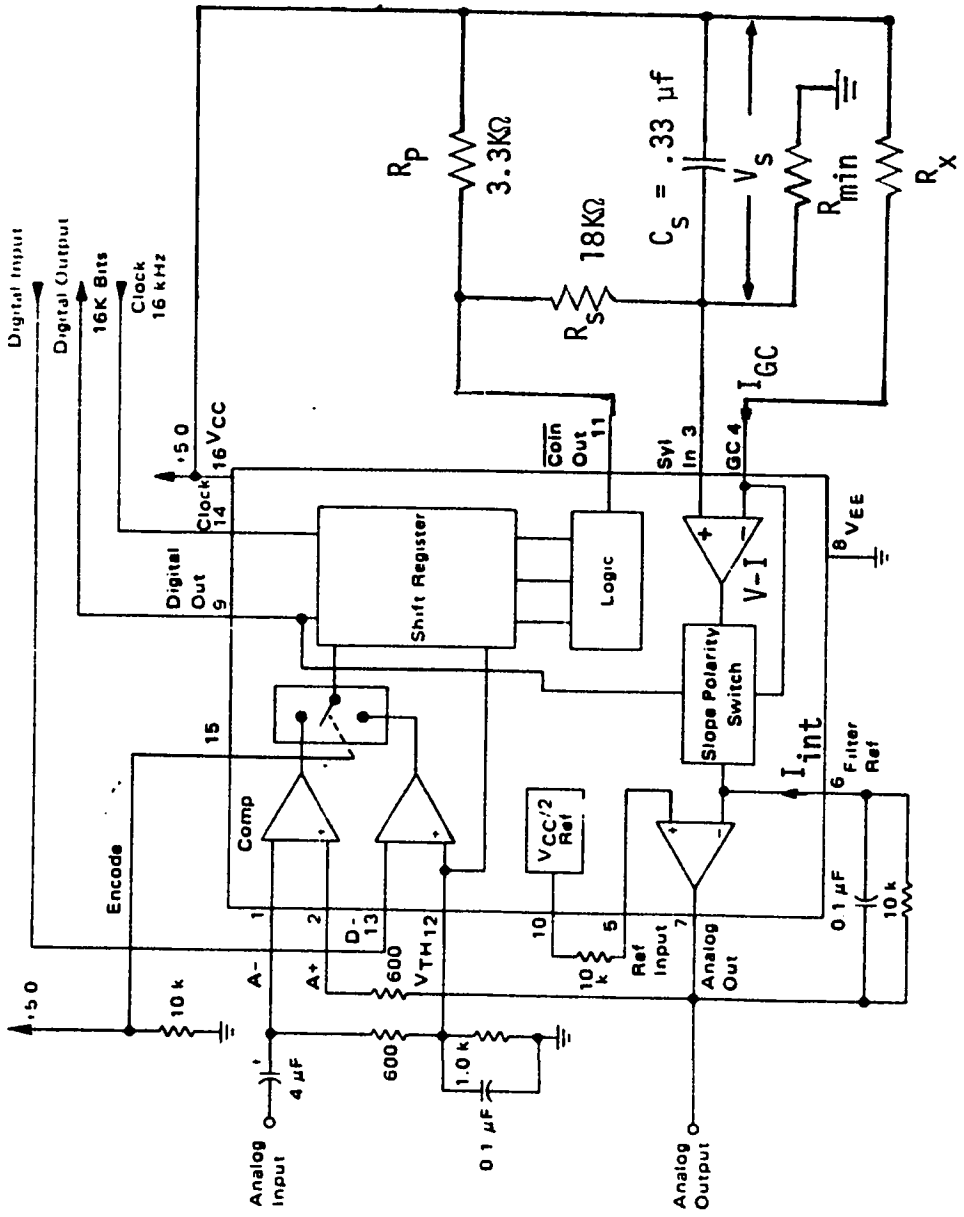


Fig. 4-10 - A CVSD encoder using MC 3417/3418, single pole companding and single integration.

Pin No.	Description
1	Audio input. (The comparator inverting input.) May be AC or DC coupled, depending on the application.
2	Analogue feedback. (The comparator non-inverting input.) In a decoding circuit, it is not used and may be tied to $V_{CC/2}$ on pin 10.
3	Syllabic filter output connection.
4	Gain control input. This is the voltage to current (V-I) converter input.
5	Reference input. The non-inverting input of the operational amplifier used as an integrator.
6	Integrator input. The integrator input or the inverting input of the operational amplifier.
7	Analogue output. This is the integrator output (output of the operational amplifier).
8	V_{EE}. The most negative terminal of the supply voltage.
9	Digital output. This output has a voltage swing between V_{CC} and V_{EE}. It is CMOS or TTL compatible.
10	$V_{CC/2}$ output. An internal low impedence mid-supply reference is provided for use of the MC3417/18 in single supply application.
11	Inverted coincidence output. This is the inversion of the signal slope analyzer output. The voltage is high whenever the register digital outputs are all 1's or all 0's.

Pin No.	Description
12	Digital Threshold. This sets the switching threshold for pins 13,14 and 15. Usually it is connected to the $V_{CC/2}$ reference.
13	Digital data input. In a decode application, the digital data stream is applied to this pin. In an encoder it is unused.
14	Clock input. The signal to establish the sampling frequency is connected to this pin.
15	Encode/decode. This allows use of the IC as an encoder/decoder; i.e. half-duplex operation. If it is at a high level, it functions as an encoder; otherwise it is a decoder.
16	V_{CC}. A power supply from 4.75 to 16.5 volts, between pin 8 and 16, may be used.

Table 4-2 - Function and pins definition of the Motorola device.

the voltage between V_{cc} and pin 3. During the charging period; i.e. when the coincidence output at pin 11 is high, the syllabic filter voltage V_s is:

$$V_s = V_H (1 - e^{-t/R_s C_s}) + V_s(0) \qquad (4\text{-}11)$$

Where: V_H is the high level of the logic output and $V_s(0)$ is the voltage on the capacitor C_s at t=0.

During the period when the output at pin 11 is low, the capacitor C_s decays at a time constant $(R_s + R_p)\, C_s$. This time constant can be set to any required value. For equal charging and discharging time constants, R_p should be much smaller than R_s, otherwise different discharging time constants are easily achievable. In figure 4-10 R_p is 3.3 KΩ. This choice makes the discharging time constant (7.0 msec) slightly longer than the charging time constant (6.0 msec). The active voltage to current (V-I) converter, drives pin 4 at the same voltage V_s and the current injected to pin 4 is then, the syllabic filter voltage V_s devided by a resistance R_x. This current is known as the gain control current (IGC) and is:

$$IGC = \frac{1}{R_x}\left[V_H(1 - e^{-t/R_s C_s}) + V_s(0)\right] \qquad (4\text{-}12)$$

The current IGC is fed to the integrating network through the slope polarity switch which changes its direction according to the sign of the difference of the analogue inputs at pins 1 and 2. The flow of the integrating current $I_{int}(IGC)$ is as shown in figure 4-10 when the

input at pin 1 is high with respect to the analogue feedback at pin 2. For the opposite state, the current I_{int} reverses its direction. A single integrating network in figure 4-10 uses the internally provided operational amplifier. The resistance R_x at pin 4 acts as a series resistance and is connected to the non-inverting terminal of the operational amplifier through the (V-I) converter and the slope polarity switch. The feedback capacitor C_f in figure 4-10 is 0.1 mf and is connected between pins 6 and 7 externally. The voltage V_o at the output of the integrator is:

$$V_o = \frac{1}{C} \int_0^t I_{int}\, dt + V(0) \qquad (4\text{-}13)$$

Where: V(0) is the voltage on the capacitor C_f at t=0.
Performing the integration over one period of the clock T_p, the change in V_o is:

$$\Delta V_o = \frac{\Delta T}{C} I_{int} \qquad (4\text{-}14)$$

Where: ΔT is the one clock period and ΔV_o is the change in the integrator output that occurs in ΔT.

Equation 4-14 indicates that, for a fixed sampling rate f_p, the change in the output voltage ΔV_o is controlled by the magnitude of the integrating current I_{int}. For a certain voltage V_s at the output of the syllabic filter, the integrating current I_{int} is controlled by the resistor R_x. Thus equation 4-14 can be rewritten as:

$$\Delta V_o = \frac{\Delta T}{C_f} \cdot \frac{V_s}{R_x} \qquad (4\text{-}15)$$

To satisfy a prescribed specification (maximum amplitude and frequency of the input), V_o should be chosen so that the feedback signal can trace the input signal without experiencing slope overload. Theoretical prediction of V_o, that will suite a prescribed specification, is difficult to ascertain. This is because the mathematical relationship of the companding signal at each instant is virtually impossible to attain. Experimental trial is needed to choose the appropriate values of the integrator elements C_f and R_x.

With no input signal (idle condition), the slope control algorithm is inactive; i.e. the coincidence output is at its low level V_L. Thus the voltage across C_s will decay to a value determined by the voltage devider consists of $(R_s + R_p)$ and R_{min} in figure 4-10. This value is given by:

$$V_s = \frac{V_{cc}(R_s + R_p)}{R_s + R_p + R_{min}} \qquad (4\text{-}16)$$

To set the step size at the idle condition, the value of R_{min} should be selected so that the voltage V_s across C_s results in the minimum peak-to-peak value at the output of the integrator. If ΔV_o at idling is denoted by $\Delta V_{o\ min}$, then the minimum value of $V_{s\ min}$ necessary across C_s using equation 4-15 is:

$$V_{s\ min} = \frac{C_f R_x}{\Delta T}\ \Delta V_{o\ min} \qquad (4\text{-}17)$$

Therefore if $V_s = V_{s\ min}$ in equation 4-16, then:

$$R_{min} = \frac{(V_{cc} - V_{s\ min})}{V_{s\ min}} (R_s + R_p) \qquad (4\text{-}18)$$

Figure 4-10 assumes $\Delta V_{o\ min} = 20$ mv, $C_f = 0.1$ µf and $R_x = 1.3$ KΩ, then $V_{s\ min}$ for a sampling rate of 16 KHZ is 41.6 mv and the required value for R_{min} is 2.5 MΩ assuming $V_{cc} = 5.0$V. A CVSD encoder using a Motorola device will function nearly at optimum performance around the prescribed specifications if the various parameters of the system (sampling rate, syllabic filter time constant, minimum step size and the loop gain) are established as given above.

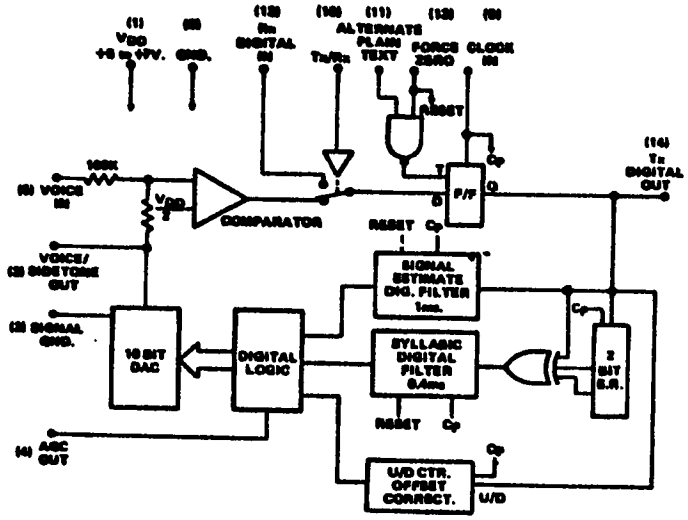
4-5.2 CVSD modulators by Harris Semiconductors Co.

Harris Semiconductors Corporation, in July 1977, marketed digital continuously variable slope delta (CVSD) modulators manufactured on a single chip.[26] The chips are half-duplex modulator/demodulator, CMOS integrated circuits. They convert voice signals into a serial of non-returning to zero (NRZ) digital data, and convert that data back into voice. The non returning to zero data is a digital representation of the binary levels where the logic output is not allowed to reach zero volt. The "1" state is represented by the high level (V_H) and the "0" state by the low level (V_L). The internal design uses digital techniques for the companding network. Digital integrators and multipliers are used to drive a 10-bit digital-to-analogue converter (DAC). The DAC output is in steps and gives a

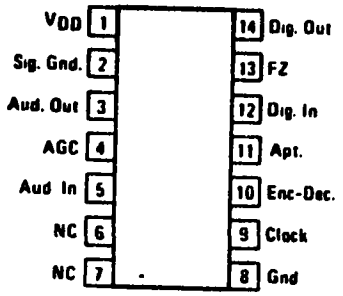
close replica of the analogue input. The time constants of the filters are automatically controlled and are proportional to the clock rates. For this reason a single device will not be optimum for all clock frequencies. Harris has two devices. The HC-55516 has internal time constants optimized for 16K-bits/sec and is useable down to 9.0K-bits/sec. The HC-55532 is optimized for 32K-bits/sec, and is useable beyond 64.0K-bits/sec. The minimum step size for the idling condition is ensured by the internal adjustment of an "up/down" counter, summed by the DAC. The approach followed in manufacturing the Harris devices allows inclusion of many desirable features which would be difficult to implement using other approaches, these include:

1) The requirement of few external parts,
2) Low power drain: 6 mw from single 5-7v supply,
3) No calibration or drift problems, automatic offset adjustment,
4) Filter reset by digital control,
5) Automatic overload recovery,
6) Automatic "quiet" (idle) pattern generation,
7) AGC control signal available.

Both units are available in 14 pins D.I.P.(HC1) or flat package (HC9) and in two temperature ranges; $-55^{o}C$ to $+125^{o}C$ and $-40^{o}C$ to $+85^{o}C$. The functional diagram and the pin layout are shown in figure 4-11. The maximum ratings and electrical characteristics for the Harris devices are given in appendix-3b.



a) Functional block diagram.



b) Pin layout.

Fig. 4-11 - Harris CVSD IC System.

Pin No.	Symbol	Description
1	V_{DD}	Positive supply voltage +5.0V to +7.0V is applied at this pin.
2	Sig. Gnd	Ground connection to D/A ladders and comparator; i.e. audio ground.
3	Aud.out	The recovered audio is taken at this pin.
4	AGC	A Logic "Low" level will appear at this output when the recovered signal excursion reaches one-half of the full scale value.
5	Aud. In	Audio input should be externally AC coupled.
6,7		No internal connection is made to these pins.
8	Gnd	Ground or negative supply voltage should be connected to this pin.
9	Clock	Sampling frequency is applied at this pin.
10	Encode/ Decode	The encode/decode functions are selected by the logic level applied to this input. A low level selects the encode mode, a high level, the decode mode.

Pin No.	Symbol	Description
11	APT	The active level is "low". It causes an "alternate plain text" (quieting pattern) to be transmitted without affecting the internal operation of the CVSD. Usually it is kept at "high" level.
12	Dig. In	The digital data is applied at this pin when used as a decoder.
13	FZ	The active level is "low". It forces the transmitted output, the internal logic, and the recovered audio output into the "quieting" condition.
14	Dig. out	The transmitted digital data is obtained at this pin.

Table 4-3 - Function and pins definition of the Harris device.

Figure 4-11 shows the internal parts of the Harris device. The forward path consists of an analogue comparator using an operational amplifier and a D-type flip flop to sample the quantized signal at the output of the comparator. The comparator inputs present a 100 KΩ in series with $V_{DD/2}$ as zero signal reference. The feedback loop consists of a two bit shift register, a 3 input exclusive OR gate, two digital filters with time constants of 1 msec and 4.0 msec acting as signal estimate filter and syllabic filter, respectively. The feedback loop also includes an up/down counter, a digital multiplier and a 10-bit digital-to-analogue converter (DAC). The manufacturer in his published pamphlet does not indicate details of these digital networks or even the type of signal driving the digital-to-analogue converter. A paper treating this device only defines the digital filter as a single pole, recursive type using shift registers with feedback |11|.

An analogue type CVSD system, which closely parallels the Harris device, is shown in figure 4-12 |11|. The system has two loops in its feedback path. The first loop has a signal estimate filter (Integrator) and a multiplier. The signal estimate filter integrates the digital output pattern to form the feedback signal y(t). The second loop has the companding network; i.e. the shift register algorithm and the syllabic filter. The companding network is active only when there is at least three or more consecutive one's or zero's in the digital pattern |11|. At idling or with low

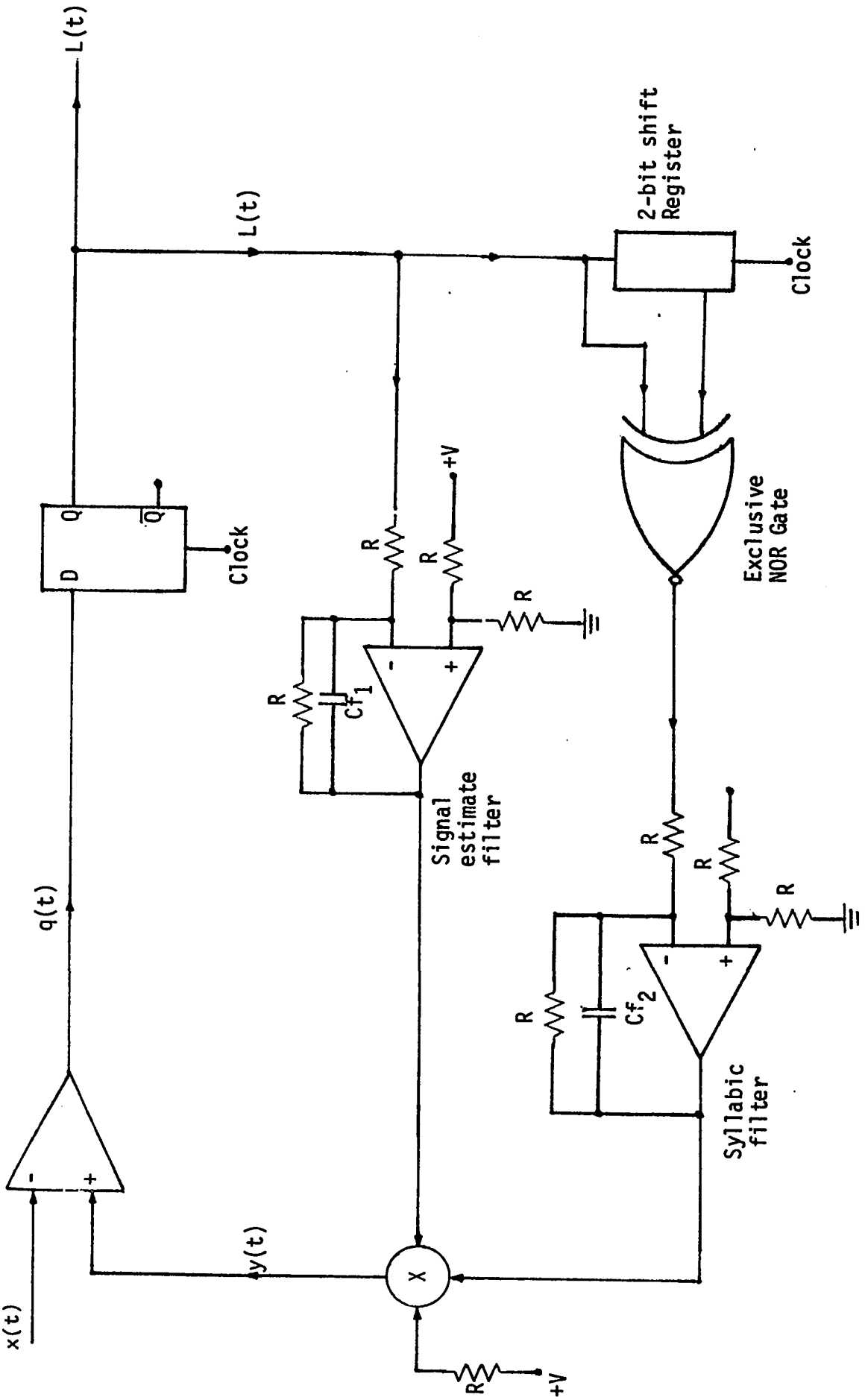


Fig. 4-12 - An analogue CVSD system which functions similarly to the Harris digital device.

input signals, the companding network is inactive. This is because at idling there are no consecutive one's or zero's at the output of the encoder. In the Harris device, the signal estimate digital filter, up/down counter, digital multiplier and the 10-bit DAC forms the first feedback loop. The shift register algorithm and the syllabic digital filter acts as the companding network. The output of the companding network is combined with that of the signal estimate filter to change the multiplier output which in turns changes the step size at the output of the DAC. In the Harris device, the output of the DAC (feedback signal) is connected internally to the analogue comparator and is available at pin 3. Since the exact nature of the signals at the output of the digital filter and at the output of the digital logic (multiplier) is not known, it is convenient to postpone the detail description of the principle of operation of this device after its practical evaluation in chapter-6.

4-6. Summary

The presentation of the two different types of integrated continuous variable slope delta modulators shows that each manufacturers followed different techniques in designing and fabricating the chips. The companding technique in the Harris device is essentially completely digital, whereas the Motorola device uses mostly analogue

elements to obtain companding signal. Harris device restricts the user on its inherent characteristics. These must be accepted, sometime resulting performance in sub-optimal performance. Basically only sampling rate, supply voltage, and the output low-pass filter need to be designed. The Motorola device provides the user with alternatives to tailor the encoder's transmission characteristics. This can be done by proper selection of the parameters controlling the output characteristics. These parameters are syllabic filter time constant, minimum step size, and the loop gain. Though this property for the Motorola device may be advantageous, a system consisting of an encoder and a decoder using Harris device is much simpler, to design and much economic. This is because, it needs very few external components and has desirable features such as automatic idling pattern generation. This has been found to aid intelligibility. The Motorola device or the conventional CVSD system shown in figure 4-6 requires precise design evaluations to attain a low noise idling pattern. Another feature of the Harris device is its automatic recovery of momentary slope overload when beginning to encode and to decode.

CHAPTER - 5

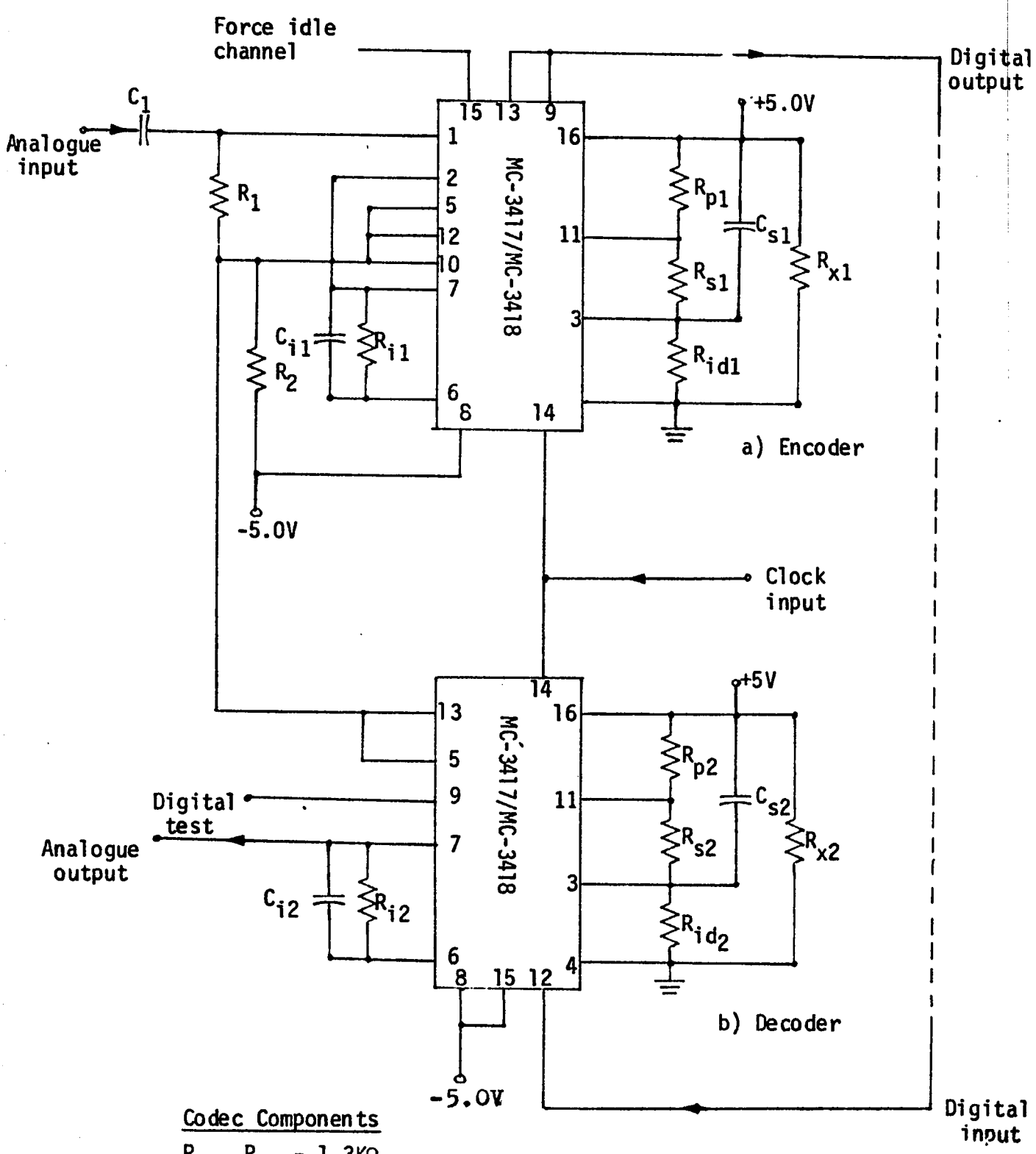
TEST RESULTS OF THE MOTOROLA CONTINUOUS VARIABLE SLOPE DELTA MODULATION SYSTEM

5-1 - Introduction

Tests, similar to those of the LDM system, were performed for the (CVSD) modulation system shown in figure 5-1. The system consists of an encoder and a decoder, both using a (CVSD) chip manufactured by the Motorola Semiconductor Corporation (MC-3417/ MC-3418). The MC-3417 device was used as a half duplex voice codec at 16.0 KHZ sampling rate. The transfer function characteristic was obtained for both devices (MC-3417 and MC-3418). This is because Motorola devices use 3-bit shift register algorithms for the MC-3417 and 4-bits algorithm for the MC-3418. The resultant transfer function characteristics are compared with theoretical predictions and shown to depend upon the shift register algorithm.

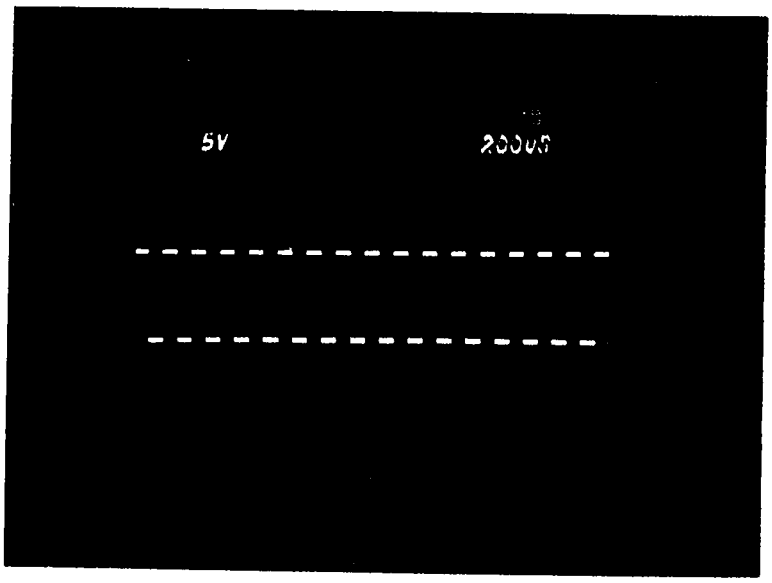
5-2 - Idling condition

The idling pattern of the (CVSD) modulation system for the MC-3417 device is shown in figure 5-2. Figure 5-3 shows this pattern in more detail. The digital output at pin 9 of the encoder (figure 5-3a) is a rectangular wave with $\pm$ 5.0V peak-to-peak (supply voltages) at a frequency of 8.0 KHZ; i.e. half the sampling rate f_p(16.0 KHZ). This is because two sampling pulses are required to generate a sequence of "1" and "0" at the output of the encoder. The binary levels; i.e. the "1" and "0" states correspond to the positive and

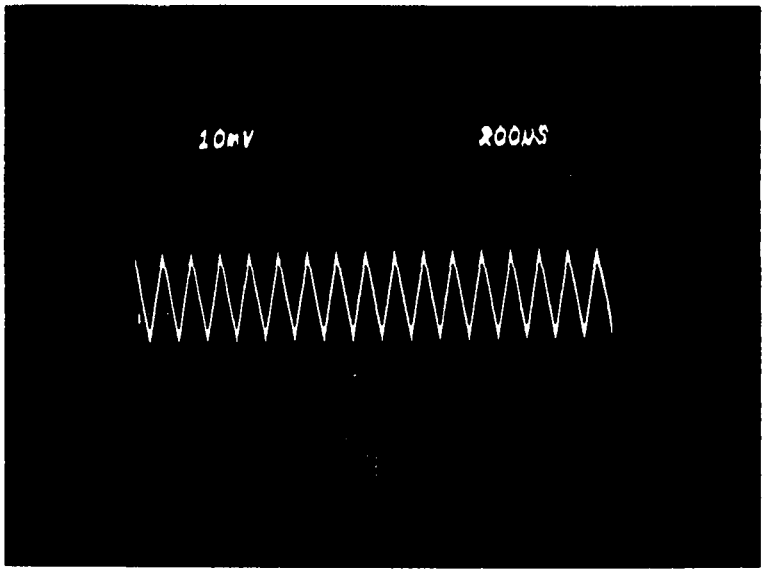


Codec Components			
R_{x1}, R_{x2}	- 1.3KΩ	R_1	- 1.0KΩ
R_{p1}, R_{p2}	- 3.3KΩ	R_2	- 1.0KΩ
R_{s1}, R_{s2}	-18.0KΩ	C_1	= 4.7 μF
R_{i1}, R_{i2}	-10.0KΩ	$C_{s1} = C_{s2}$	- 0.33 μF
R_{m1}, R_{m2}	- 2.4MΩ	$C_{i1} = C_{i2}$	- 0.1 μF

Fig.5-1 - Full duplex 16K bit voice codec using MC-3417/MC-3418.



a) Digital output.



b) Analogue output.

Fig. 5-2 - Idling pattern of the MC-3417 (CVSD) system.

the negative supply voltages, respectively. The decoded signal at idling (figure 5-3b) is a triangular wave with 20 mv peak-to-peak amplitude at half the sampling rate f_p, since it corresponds to the integral of a square wave current. The syllabic voltage V_{cs} across the capacitor C_s is a constant d.c. voltage. Its value is represented by V_{smin} and is the minimum value required to generate the idling pattern. The magnitude of V_{smin} is determined by the voltage divider consisting of $R_p + R_s$ and R_{id} in figure 5-1. The voltage to current (V/I) converter (an internal part of the Motorola chip, shown in figure 5-9) converts the syllabic voltage V_{cs} into current termed "gain control current" (I_{GC}). The magnitude of this current is given by the ratio V_{smin}/R_x (see section 5-3). This current (I_{int}) is fed to an integrating network. The direction of I_{int} is controlled by the slope polarity switch (shown in figure 5-9), according to the state of L(t) pattern. As the time duration of the "1" state is equal to that of the "0" state in the L(t) idling pattern, the integration is of a square wave current and results in a triangular waveform at the output of the decoder (pin 7).

The frequency spectrum of the decoded wave (figure 5-4) is consistent with the Fourier series expansion of a triangular wave. Figure 5-4 also shows a peak of 0.24 mv at 16.0 KHZ. This peak is due to the spikes occuring at the sampling rate and are visible in figure 5-3. Table 5-1 compares the measured peaks with those theoretically expected. The 5th and the higher harmonics were too small in amplitudes to be recorded by the spectrum analyzer.

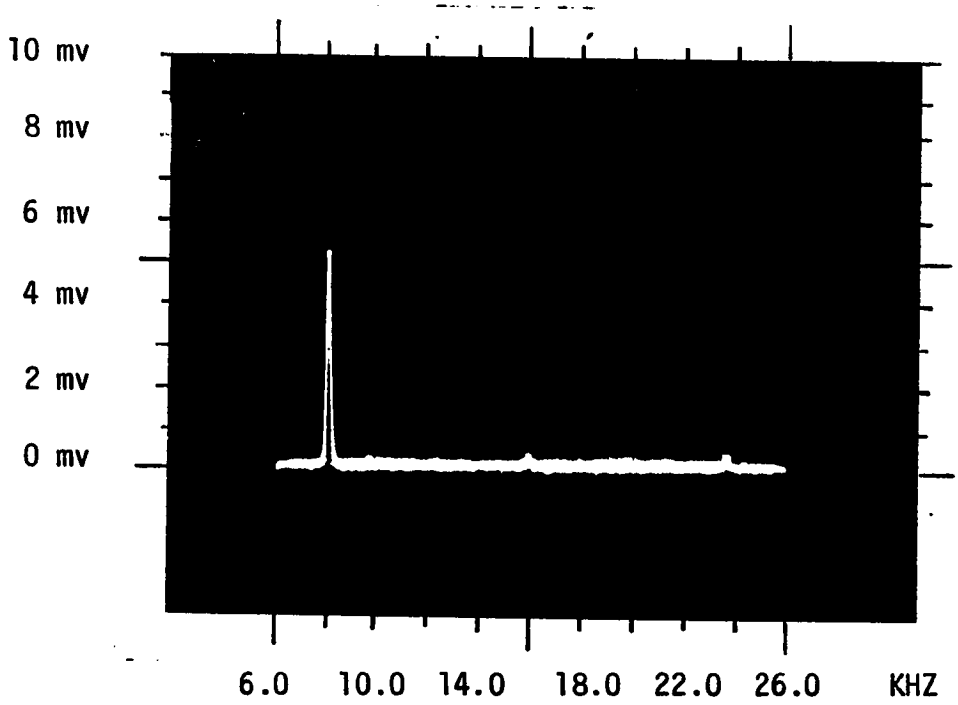


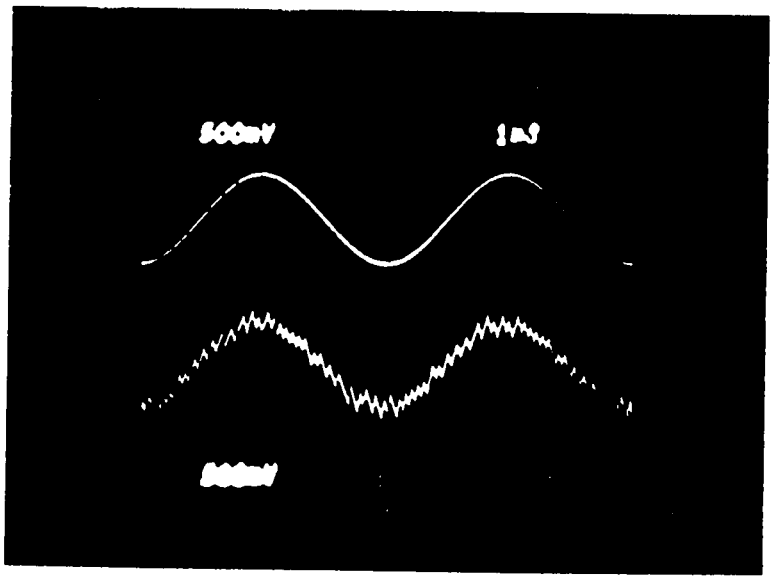
Fig. 5-4 - Frequency spectrum of the idling decoded waveform.

Peak No.	Computed peaks mv	Measured peaks mv	Frequency KHZ	% difference
1st	8.1	7.78	8.0	4.0
2nd	-	0.24	16.0	-
3rd	0.9	0.85	24.0	5.5

Table 5-1 - Computed and measured peaks of the frequency spectrum of the decoded wave at idling.

5-3 - Normal operating condition

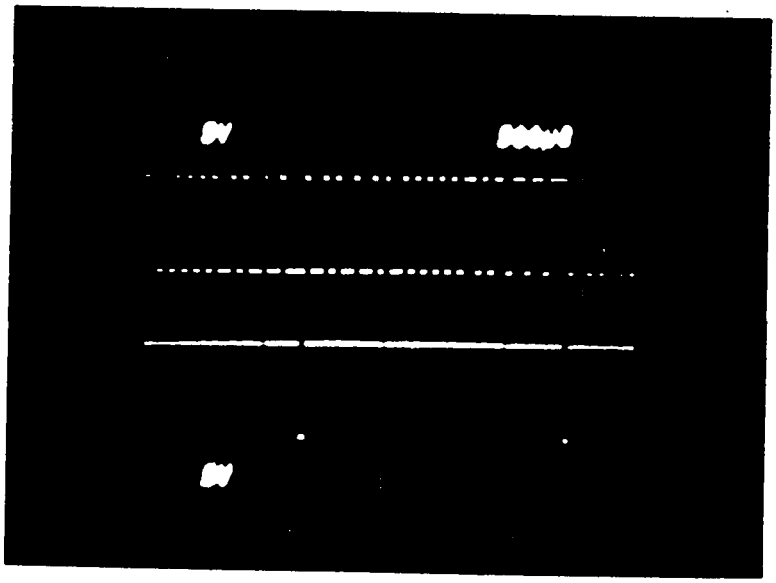
Under normal operating conditions the decoded signal of the (CVSD) system provides the decoded signal shown in figure 5-5b for a sinusoidal input. The decoded signal is a sequence of ramps, rather than of steps as it was the case for the LDM system. The digital output L(t) at pin 9 and the coincidence output at pin 11 are shown in figure 5-6. It is important to state that, the Motorola device was manufactured to give the inverted version of the signal slope analyzer; (SSA) i.e. pin 11 will be at the "1" state ($+V_{cc}$) when the (SSA) output is low and will be at the "0" state ($-V_{cc}$) when the SSA output is high. The coincidence output at pin 11 is activated; i.e. its level is changed from high to low when a certain state of L(t) pattern (either "1" or "0") persists for a time long enough to make all registers at an identical state (all "1's"or "0's".



a) Analogue input

b) Analogue decoded output

Fig. 5-5 - Decoded output of the MC-7417 (CVSD) system in normal operating condition.



a) Digital pattern L(t) at pin 9.

b) Coincidence output G(t) at pin 11.

Fig. 5-6 - Digital pattern L(t) and coincidence output G(t) under normal operating condition.

Figure 5-7 illustrates that for a shift register with "n" registers, the least number of pulses required to make the n registers at identical state is n pulses. The figure also indicates that the time interval for n consecutive pulses is $(n-1)T_p$. Where T_p is the reciprocal of the sampling rate f_p. Figure 5-6b shows that this time interval is 125 μsec. This is equivalent to $2T_p$ for a sampling rate of 16 KHZ and n=3 (MC-3417 device uses 3-bit registers in SSA algorithm). For a condition of figure 5-5a, this is shown twice in figure 5-6, once at three consecutive "0's"and once at three consecutive "1's". The syllabically controlled signal at pin 3 is shown in figure 5-8b. The following analysis is necessary to understand how this signal is obtained from the state of the coincidence output at pin 11. Figure 5-9 shows a portion of the internal circuitry of the MC-3417/MC-3418 devices and an external circuit necessary to control the feedback companding network. The loading effect of the V/I converter (figure 5-9) can be analyzed by considering incremental changes of node voltages V_3 and V_4. The change in the output voltage V_o at the output of operational amplifier is given by:

$$\Delta V_o = A_v(\Delta V_3 - \Delta V_o) \qquad A_v > 0 \qquad (5\text{-}1)$$

The equivalent circuit of the emitter follower stage (Q_1 & Q_2) at the output of the operational amplifier is shown in figure 5-9b.

Shift registers states.

Pulse No.	Q_4	Q_3	Q_2	Q_1	Q_o
1st	1	0	0	0	0
2nd	1	1	0	0	0
3rd	1	1	1	0	0
4th	1	1	1	1	0
5th	1	1	1	1	1

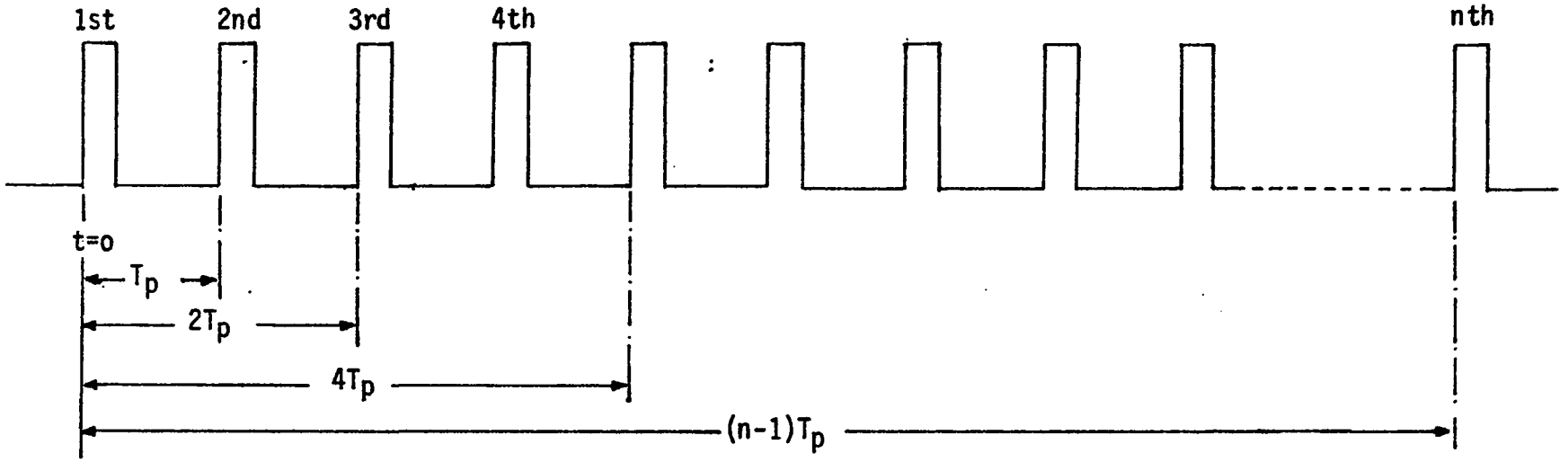
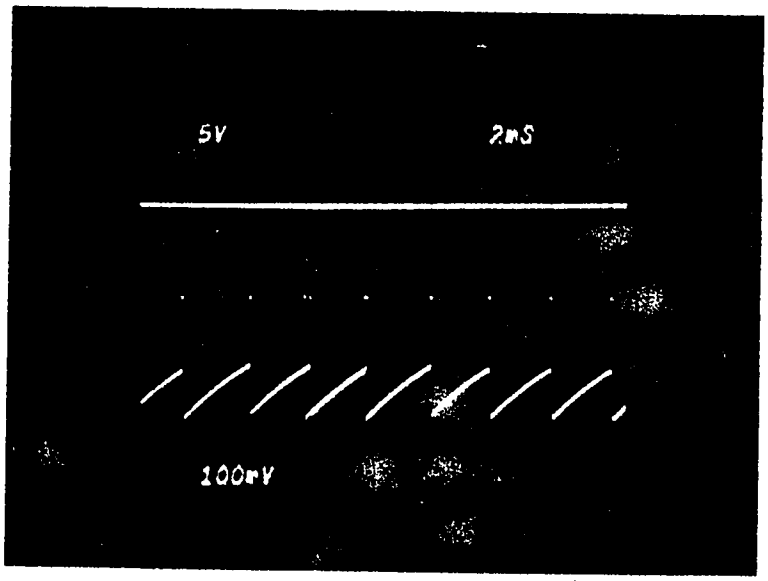


Figure 5-7 - An illustration showing that the time interval for n consecutive pulses is given by $(n-1)T_p$. The figure assumes n shift registers.



a) Coincidence output G(t) at pin 11.

b) Syllabically controlled signal at pin 3.

Fig. 5-8 - Behaviour of the syllabically controlled signal under normal operating condition.

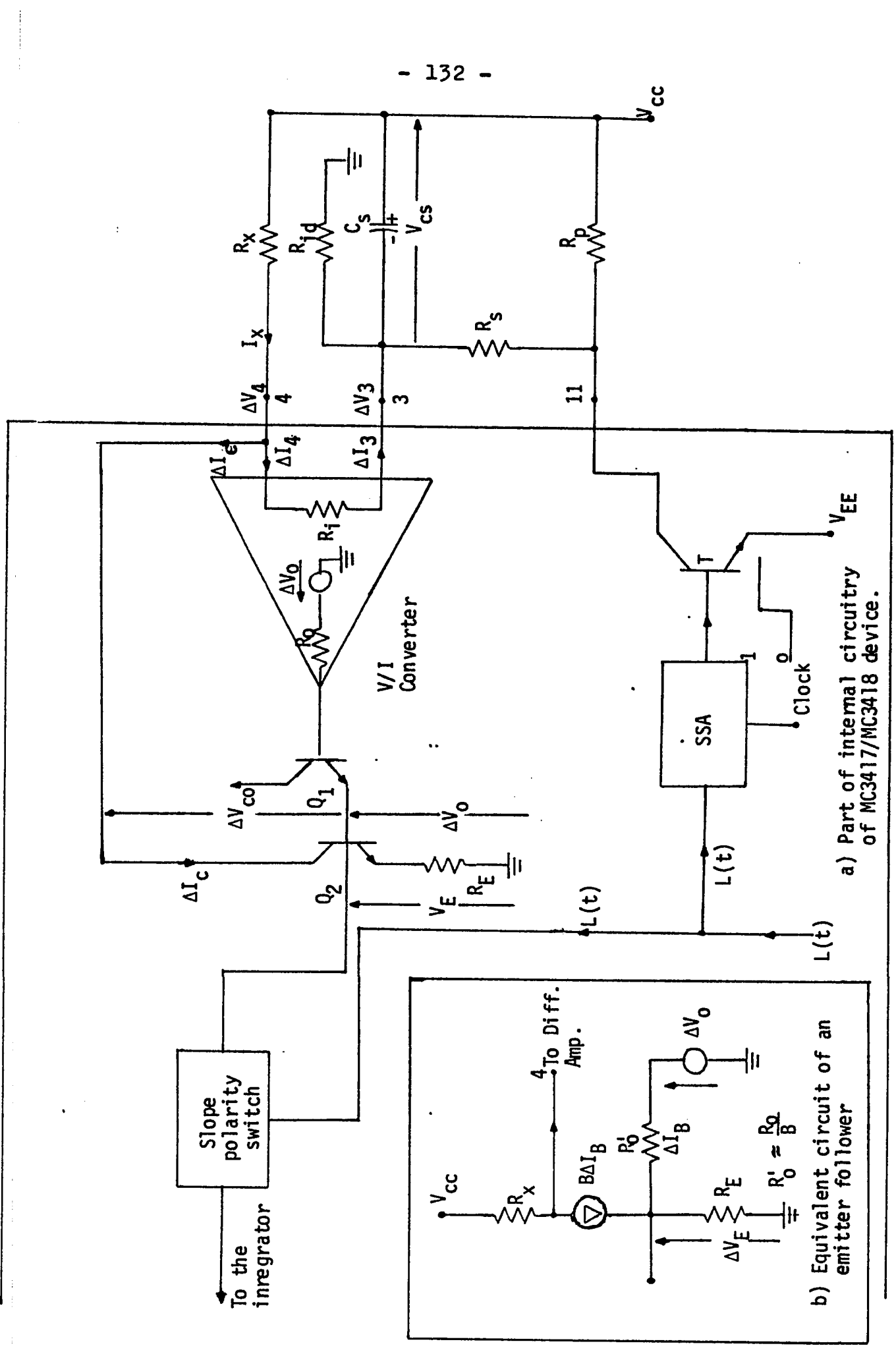


Fig. 5-9 - Single pole syllabic filter and loop gain controlling resistance R_x connected externally to the MC3417/MC3418 device.

Assuming $\beta R_E >> R_o$, then for the emitter follower $V_E \simeq \Delta V_o$, and:

$$\Delta I_c = \beta \Delta I_B \simeq \frac{\Delta V_o}{R_E} = \frac{A_v(\Delta V_3 - \Delta V_4)}{R_E} \qquad (5\text{-}2)$$

For any dynamic change at node 3 and 4, the change in the current I_4 is given by:

$$\Delta I_4 = \frac{\Delta V_4 - \Delta V_3}{R_i} \qquad (5\text{-}3)$$

Expressing ΔI_4 in terms of ΔI_c from equation 5-2:

$$\Delta I_4 = \frac{R_E}{R_i} \cdot \frac{1}{A_v} \cdot \Delta I_c \qquad (5\text{-}4)$$

The approximate input resistance R_i of the V/I converter, from the schematic of the Motorola device (see figure A6-1), is $R_i (= 2r_{dN} + 2\beta r_{dp}) \simeq 100K\Omega$. Since usually $A_v \geq 1000$, then in equation 5-4, $\Delta I_4 << \Delta I_c$. Furthermore, $\Delta I_x = \Delta I_c + \Delta I_4$, then $\Delta I_x \simeq \Delta I_c$.

The above analysis indicates that the V/I converter has essentially no loading effect on the externally connected circuit at pins 3 and 4. It also shows that since $I_4 = I_3 \simeq 0$, the voltage drop across R_i is nearly zero; i.e. the node voltages $V_3 \simeq V_4$. The current I_x which is termed as "gain control current " (I_{Gc}) now can be written as:

$$I_{Gc} = \frac{V_{cc} - V_4}{R_x} \simeq \frac{V_{cc} - V_3}{R_x} = \frac{V_{cs}}{R_x} \qquad (5\text{-}5)$$

Since: $V_3 = V_{cc} - V_{cs}$

The current I_{Gc} is fed to the integrating network through the slope polarity switch; i.e. $|I_{int}| \simeq I_{Gc} = \frac{V_{cs}}{R_x}$. The integral of I_{int} provides a rampwise decoded signal at pin 7.

Figure 5-9 shows that when the SSA output is high, transistor T is "ON". Pin 11 for this condition is at the level of V_{EE}. This corresponds to the low state of the coincidence output. Relevant portions of the external circuit are shown in figure 5-10a. Capacitor C_s is charged with a time constant given by $(R_s//R_{id})C_s$. Since $R_{id} >> R_s$, the charging time constant is approximately R_sC_s. The node voltage at pin 3 (V_{Rid}) at any instant is given by:

$$V_{Rid}(t) = V_{cc} - V_{cs}(t) \quad (5\text{-}6)$$

OR:

$$V_{Rid}(t) = V_{Rs}(t) - V_{cc} \quad (5\text{-}7)$$

By equating equations 5-1 and 5-2 one has that at any instant:

$$V_{cs}(t) + V_{Rs}(t) = 2V_{cc} \quad (5\text{-}8)$$

Furthermore:

$$V_{cs}(t) = \left[2V_{cc} - V_{sR}(Min)\right] (1-e^{-t/\tau_1}) + V_{cs}(0)\, e^{-t/\tau_1} \quad (5\text{-}9)$$

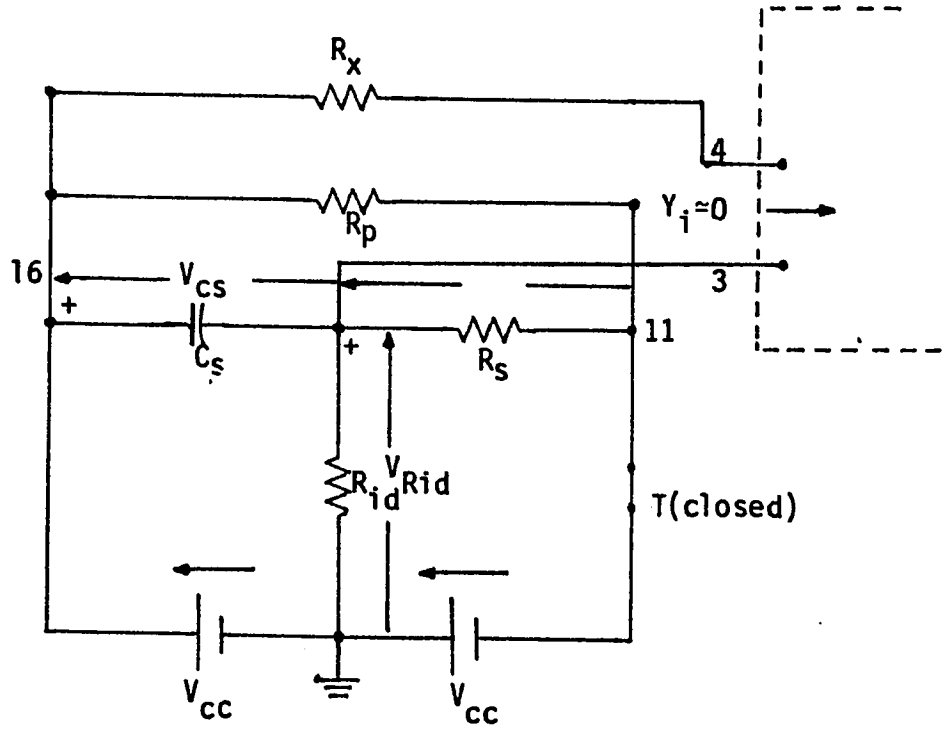


Fig.5-10a - External circuit at low condition of the coincidence output.

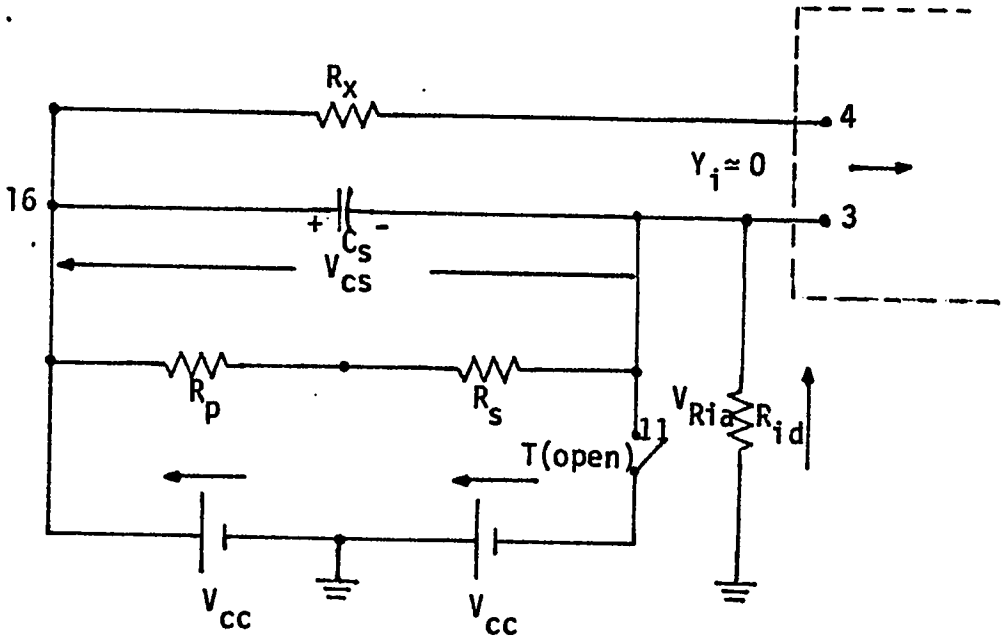


Fig.5-10b - External circuit at high state of the coincidence output.

Where:

$$\tau_1 = (R_s // R_{id})C_s \simeq R_s C_s$$

$V_{cs}(0)$ is the voltage on capacitor C_s at t=0

$V_{sR}(Min)$ is the voltage drop across R_s at steady state.

The magnitude of $V_{Rs}(Min)$ from loop (3-11-G) is:

$$V_{Rs}(Min) = \frac{V_{cc}}{R_s + R_{id}} \cdot R_s \qquad (5\text{-}10)$$

Substituting the value of $V_{cs}(t)$ from equation 5-9 into equation 5-6, the instantaneous node voltage at pin 3; i.e. across R_{id} is:

$$V_{Rid}(t) = \left[2V_{cc} - V_{sR}(Min) - V_{cs}(0)\right] e^{-t/\tau_1} - \left[V_{cc} - V_{sR}(Min)\right] \qquad (5\text{-}11)$$

When the SSA output is low, transistor T in figure 5-9 is "off", pin 11 is driven to V_{cc}. For this condition, the external circuit shown in figure 5-10b is applicable. Capacitor C_s discharges with a time constant $\tau_2 = \left[(R_p + R_s) // R_{id}\right]C_s$. Since $R_{id} >> R_s + R_p$, the discharging time constant is $\tau_2 \simeq (R_p + R_s)C_s$. At any instant during the discharging period, the summation of the voltages across C_s and R_{id} is equal to $+V_{cc}$; i.e.:

$$V_{cs}(t) + V_{Rid}(t) = V_{cc} \qquad (5\text{-}12)$$

At steady state the voltage across C_s is at its minimum value; i.e.:

$$V_{cs}(Min) = \frac{V_{cc}(R_p + R_s)}{R_p + R_s + R_{id}} \qquad (5\text{-}13)$$

The instantaneous voltage across C_s during the discharging period can therefore be written as:

$$V_{cs}(t) = V_{cs}\, e^{-t/\tau_2} + V_{cs}(Min)(1 - e^{-t/\tau_2}) \qquad (5\text{-}14)$$

Where:

$$\tau_2 = \left[(R_p + R_s) \,//\, R_{id}\right] C_s \simeq (R_p + R_s) C_s$$

V_{cs} is the voltage stored on C_s during the charging period.

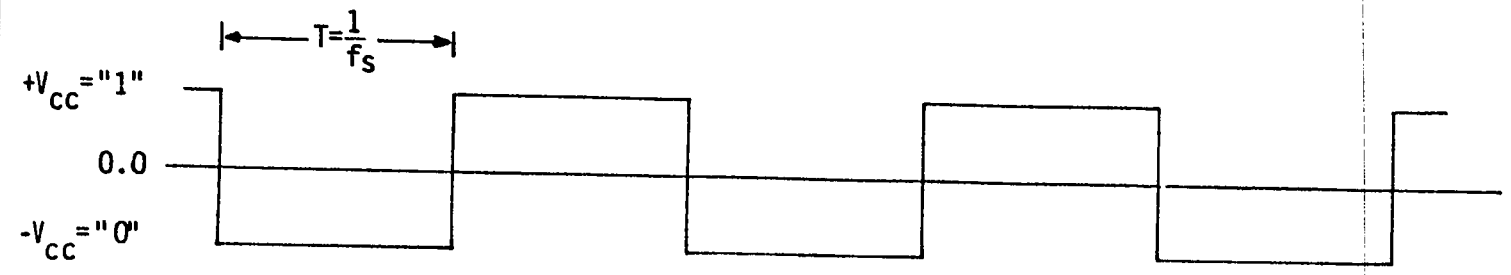
And the voltage across R_{id} is then:

$$V_{Rid}(t) = V_{cc} - V_{cs}(t) \qquad (5\text{-}15)$$

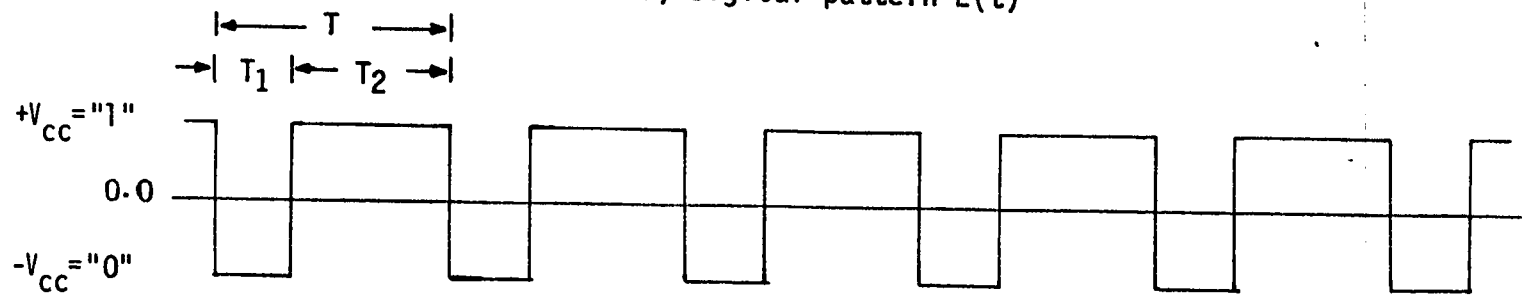
Equations 5-11 and 5-15 represent the voltage shown in figure 5-8b, since this signal was monitored at node 3.

Figure 5-11 illustrates the digital pattern L(t), the SSA output G(t), the coincidence output $\overline{G(t)}$ at pin 11, and the syllabically controlled voltage across C_s and R_{id} corresponding to the preceding analysis.

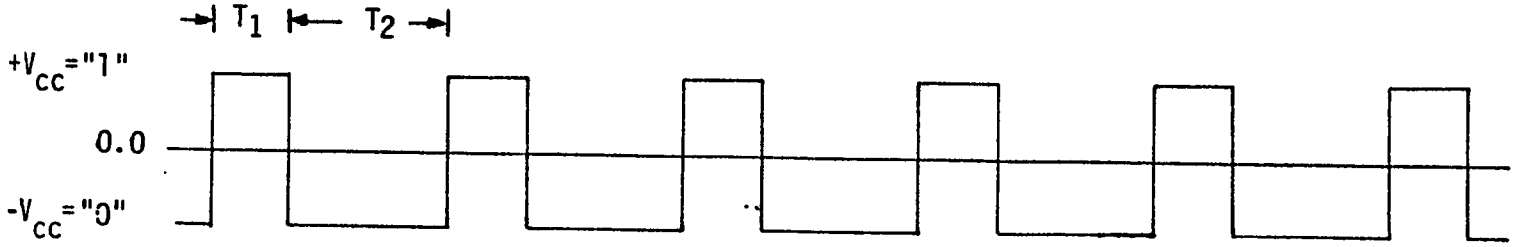
The frequency spectrum of the decoded wave is shown in figure 5-12. Figure 5-13 shows the noise within the spectrum more vividly. An average amplitude of 12 mv over a frequency band from 250 HZ to 10.0 KHZ is shown in this figure. By sampling the same analogue signal once at f_p = 8.0 KHZ and once at f_p = 32.0 KHZ, the effect of changing the sampling rate on the spectrum of the decoded signal is shown in figures 5-14 and 5-15, respectively. The lower sampling rate shows irregular distribution of the noise (figure 5-14) over a frequency band from 500 HZ to 6.0 KHZ. Peaks of approximately 30 mv are seen in this figure. With a higher sampling rate (figure 5-15) the frequency range is wider (500 - 20 KHZ) and the amplitude of the noise is smaller than that obtained at f_p = 8.0 KHZ or 16.0 KHZ. An average distribution of 5.0 mv can be assumed over the span of 20 KHZ. Reconstruction of the analogue signal in ramps instead of steps has the advantage of reducing



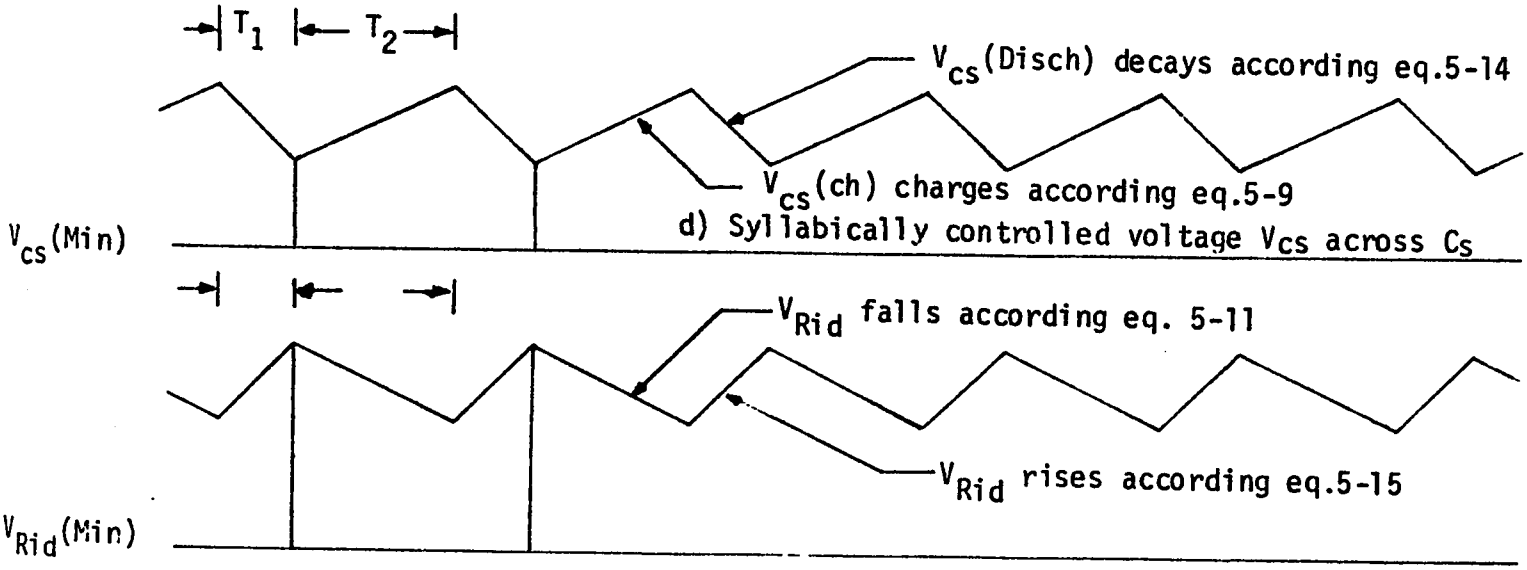
a) Digital pattern L(t)



b) Signal slope analyzer output G(t)



c) Coincidence output at pin 11 $\overline{G(t)}$



e) Syllabically controlled voltage at pin 3.

Fig. 5-11 - Determination of the syllabic voltage v_{cs} from L(t).

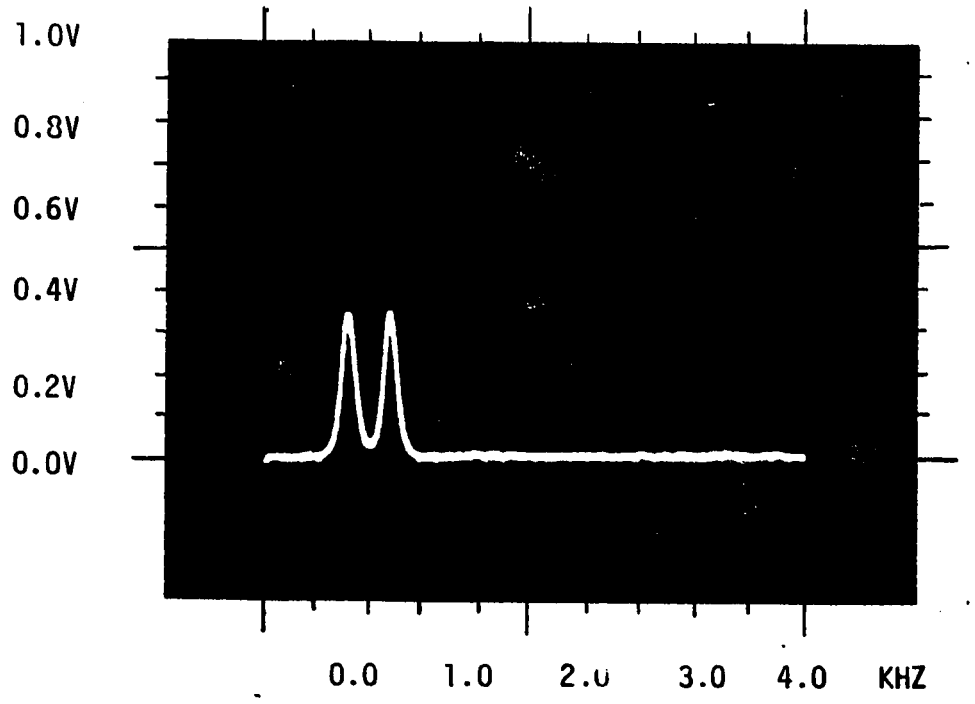


Fig. 5-12 - Frequency spectrum of the decoded wave under normal operating condition.

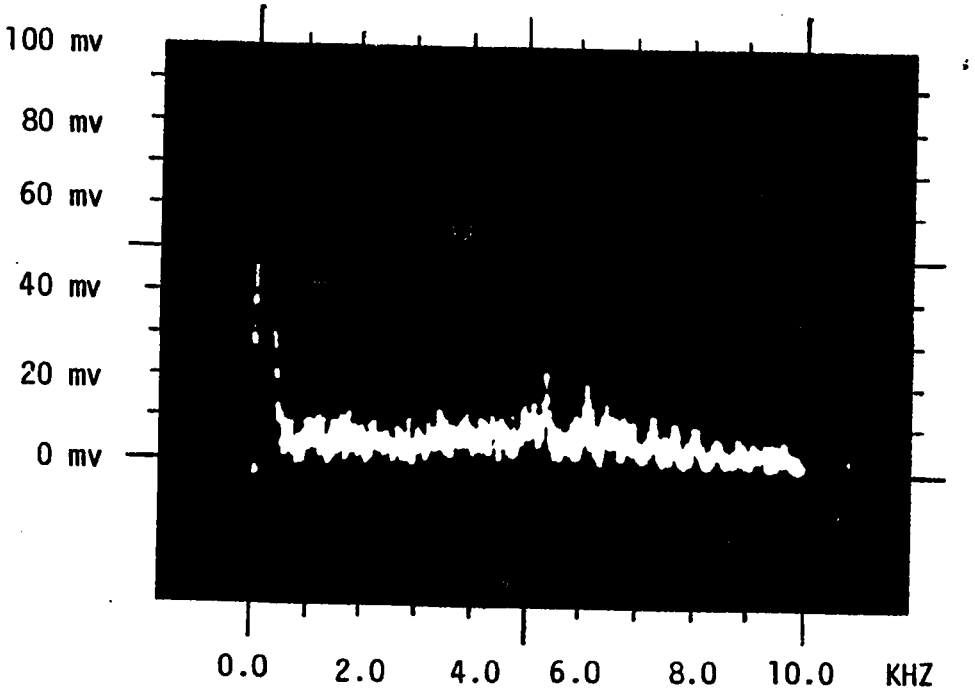


Fig.5-13 - Quantization noise at f_p=16.0 KHZ. System in normal operating condition.

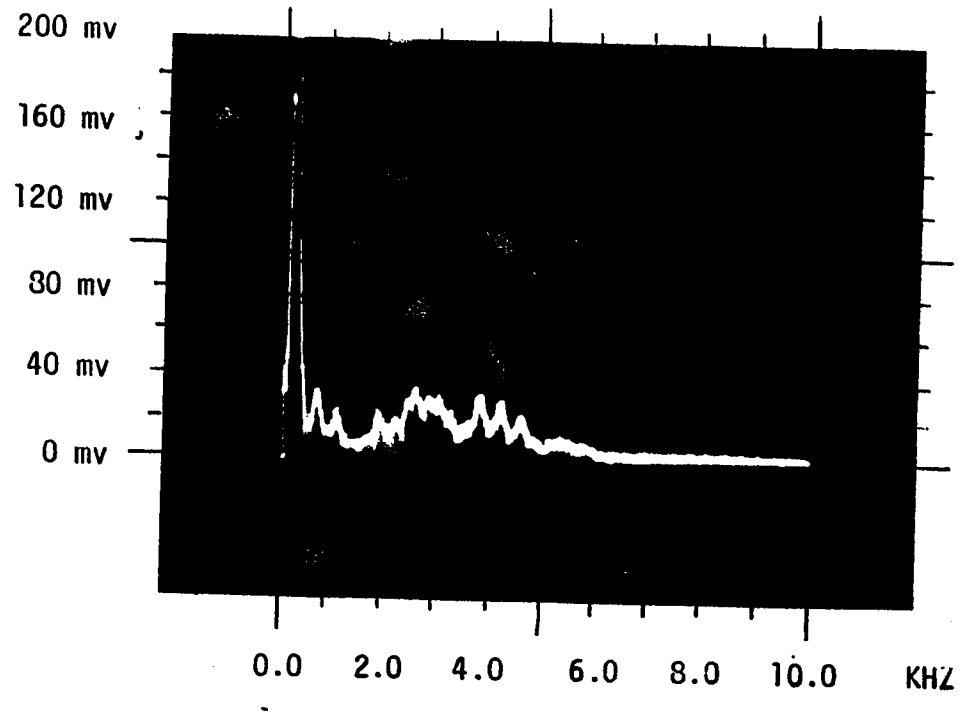


Fig.5-14 - Quantization noise at f_p=8.0 KHZ. System in normal operating condition.

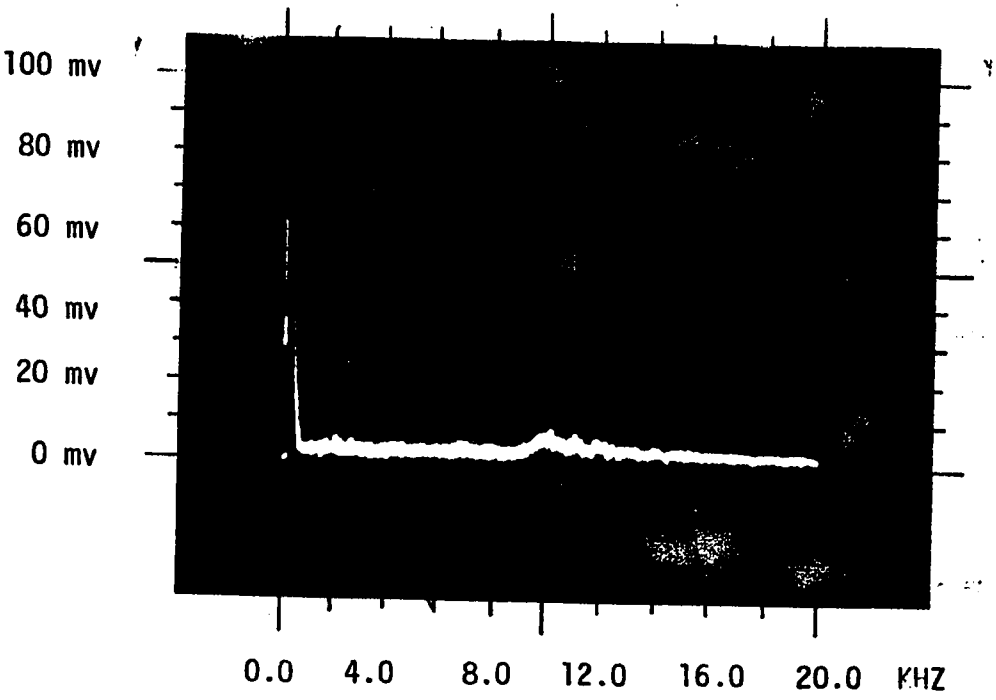
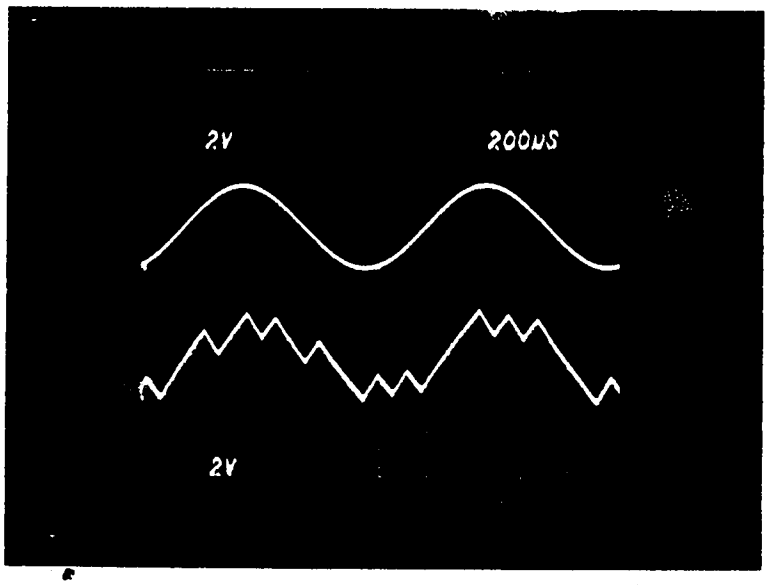


Fig.5-15 - Quantization noise at f_p=32.0 KHZ. System in normal operating condition.

the error between the two input signals at the comparator inputs. Consequently, this leads to less noise. Although the reconstruction is not in steps; i.e. possesses continuity, each successive rise extends over a predetermined increment. In a sense, quantization occurs. Therefore, the noise arising from the piecewise linear (ramp) approximation of a signal is tantamount the quantization noise.

5-4 - Slope overloading condition

By increasing the frequency of the input signal shown in figure 5-5a, a condition is reacted (figure 5-16a) where consecutive numbers of "1's"and "0's"are developed in the L(t) pattern. Under this condition, the companding network is activated and consequently the gain of the feedback loop is varied according to the slope variation of the input signal. The system is able to track the input, but for the portions where the rate of increase/decrease of the input sinusoidal signal is greater than that of the locally decoded signal. The system can be said to experience partial slope overloading condition. At maxima and minima, where the slope of the sinusoidal input is small, the decoded signal oscillates in ramps until the slope of the input is again greater than that of the locally decoded signal. Such condition may be named as partially



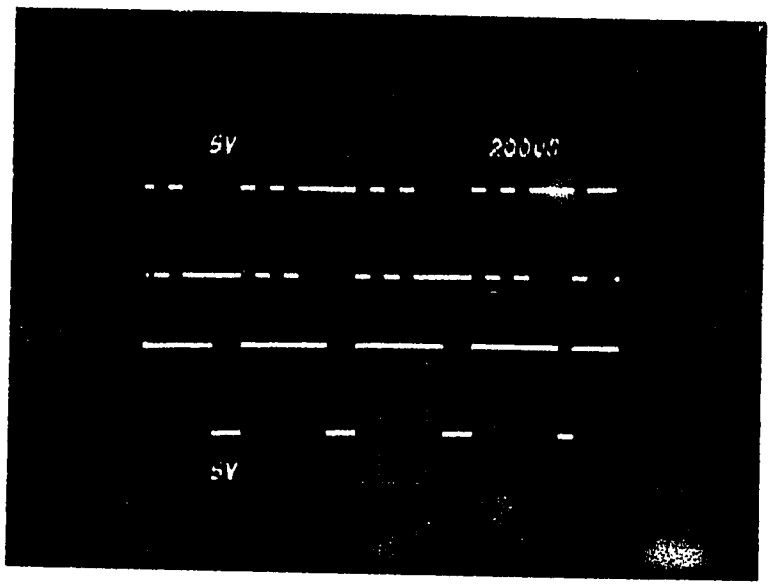
Analogue input

Decoded waveform

Fig.5-16 - Response of the MC-3417 (CVSD) system in partially slope overloaded condition.

slope-overloading condition. The decoded signal for this condition is shown in figure 5-16b. The digital pattern L(t), during the partially slope-overloading region is either in the "1" or in the "0" state according to the sign of the rate of the input signal. In the hunting region a sequence of "1's"and "0's"are generated. This is shown in figure 5-17a. Figure 5-17b, shows the coincidence output at pin 11. It has the "1" state as long as L(t) has a duration less than $2T_p$; i.e. 125.0 μsec at f_p = 16.0 KHZ. For a periodic input signal, the fundamental frequency of the L(t) pattern is the same as that of the input. The coincidence output signal has a fundamental at twice the input frequency. This is because the coincidence output is activated once for the consecutive "1's" and once for the consecutive "0's". The integration of the converted current from the syllabic voltage V_{cs}, produces the decoded rampwise wave (figure 5-16b).

The frequency spectrum of the decoded wave at partially slope-overloading condition is shown in figure 5-18. The figure shows a dominant peak at the fundamental frequency and smaller peaks for the noise spectrum. The noise for this condition is in two types, side-band harmonics, at odd multiples of the fundamental frequency, and quantization noise. The side-band harmonics are due to the ramp arising from the partially slope-overloading portions (which constitutesatriangular wave at the fundamental frequency). The quantization noise is due to the quantized error



a) Digital pattern L(t) at pin 9.

b) Coincidence output at pin 11.

Fig.5-17 - Behaviour of the digital pattern at the output of the encoder. System partially slope overloaded.

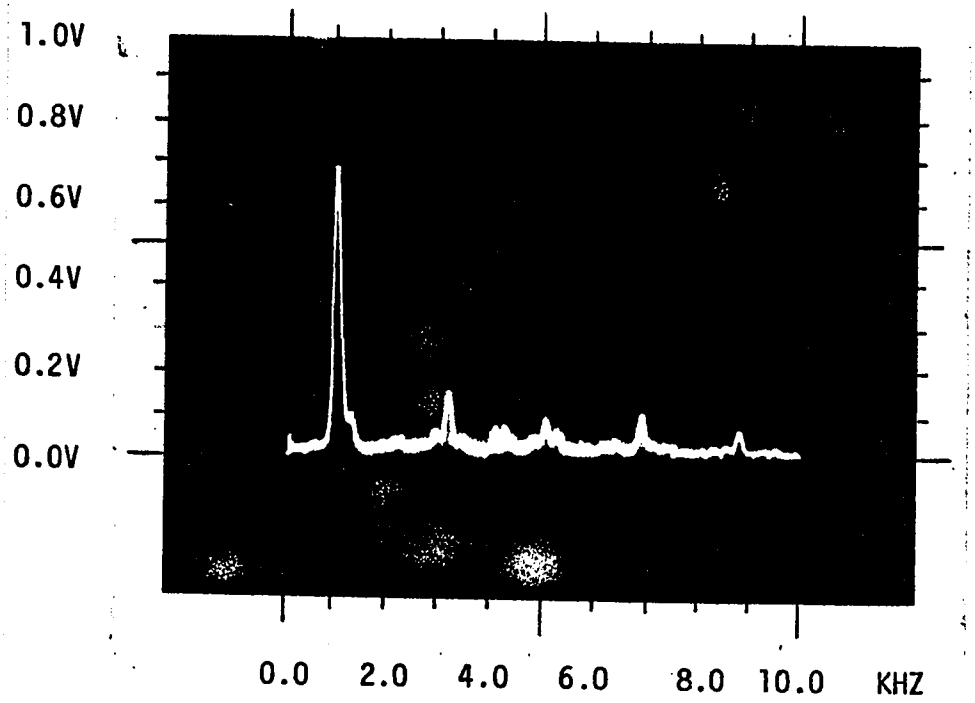
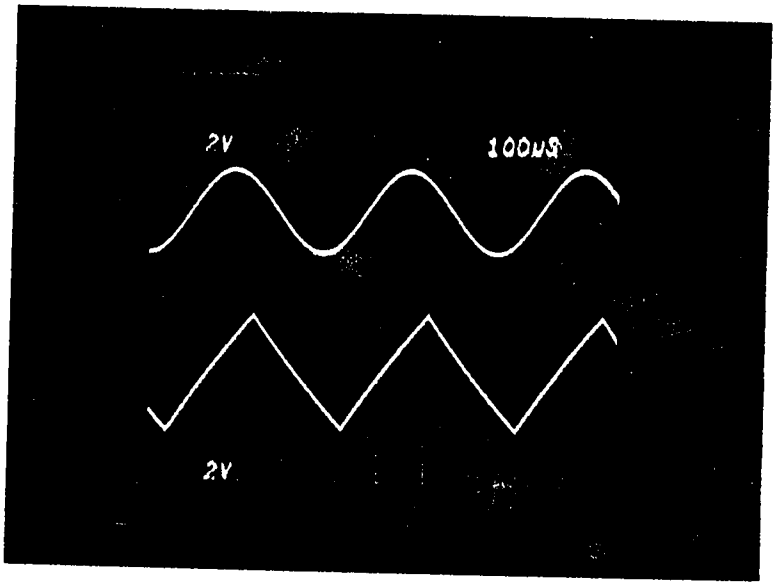


Fig.5-18 - Frequency spectrum of the decoded wave. System partially slope overloaded.

resulting from the difference between the analogue input signal and the rampwise decoded signal at the hunting portions. No doubt, the noise under this condition is higher than that of the normal operating condition (section 5-3), but a companded system tends to provide approximately a constant signal-to-noise ratio over a wider range of amplitudes or frequencies of the input signal. This is due to the variation of feedback gain to assist in tracking.

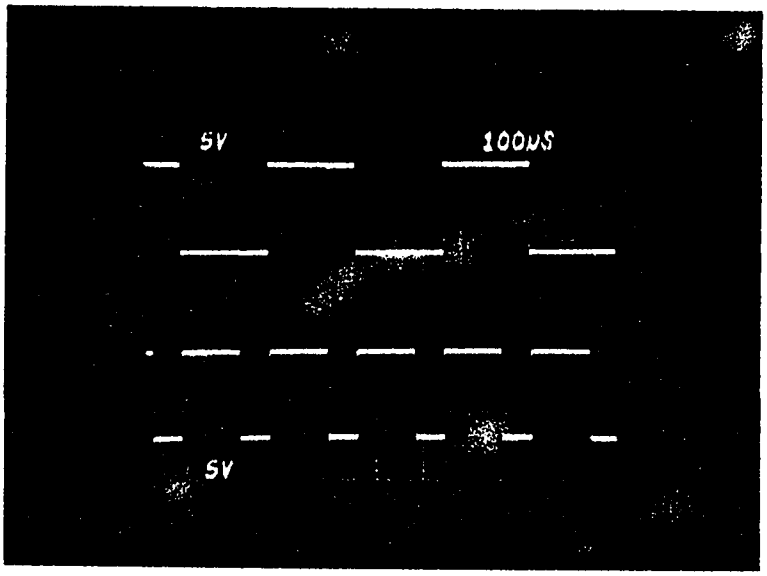
By further increasing the frequency of the input signal, (figure 5-19a) a condition is reached where the decoded wave is essentially totally triangular (figure 5-19b). The system for this condition is called as "completely" or "grossly" slope-overloaded. The digital pattern L(t) for one cycle of the input (figure 5-20a) has equal time durations for the "1" and the "0" state. It alternates at the frequency of the input signal. The coincidence output (figure 5-20b), changes its state from "1" to "0" after the time period of three consecutive "1's"or "0's"state. This signal is shown more vividly in figure 5-21a. The syllabically controlled node voltage at pin 3 is shown in figure 5-21b. Integration of the current (I_{int}), from the V/I converter, results in the triangular waveform as shown in figure 5-19b. At the grossly slope-overloaded condition, a phase shift angle (ϕ) is introduced between the analogue input and the decoded triangular wave. The magnitude of phase shift angle ϕ depends upon the time constant of the feedback integrator. It is directly proportional to the time constant. Figure 5-22 indicates that the magnitude of ϕ at this condition is approximately 70^{o}.



a) Analogue input

b) Decoded output

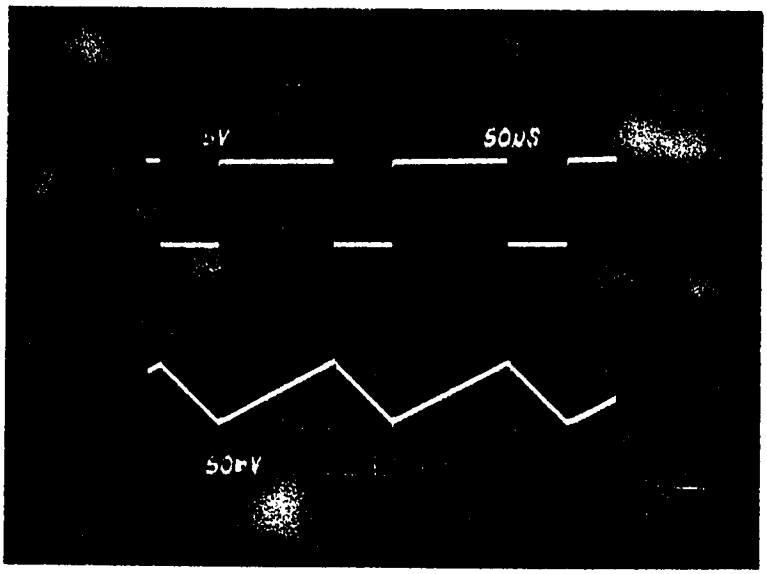
Fig.5-19 - Response of the MC-3417 (CVSD) system under grossly slope overloading condition.



a) Digital output L(t) at pin 9.

b) Coincidence output at pin 11.

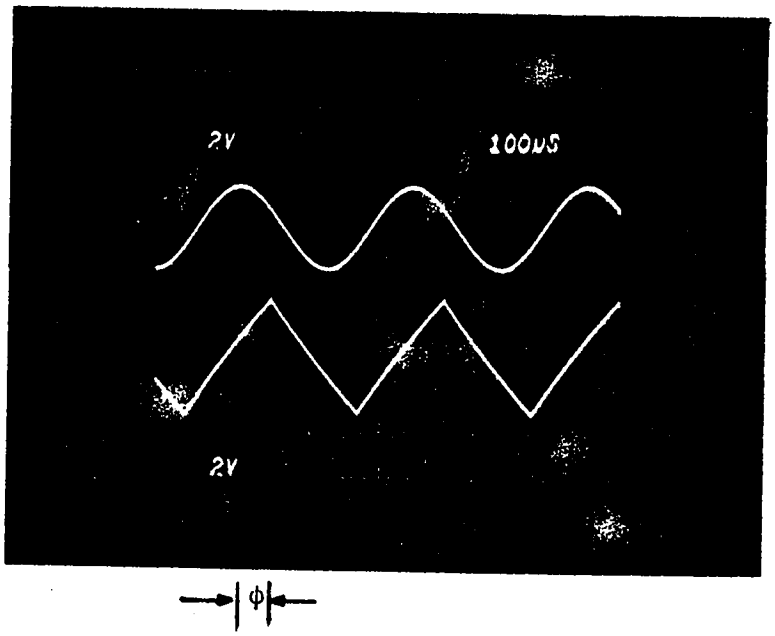
Fig.5-20 - Digital pattern at the output of MC-3417 encoder at grossly slope overloading condition.



a) Coincidence output at pin 11.

b) Syllabically controlled signal at pin 3.

Fig.5-21 - Nature of the syllabically controlled signal at pin 3 for grossly slope overloaded condition.



a) Analogue input

b) Triangular decoded wave

Fig.5-22 - Triangular decoded wave shifted by an angle ϕ. System under grossly slope overloaded condition.

The frequency spectrum of the triangular decoded wave (figures 5-23 and 5-24) show the fundamental and its odd harmonics. The measured peaks and the theoretically expected peaksare given in table 5-2.

n	Computed peak V	Measured peak V	Frequency KHZ	% difference w.r.t. the computed
1	1.42	1.53	2.7	7.7
3	0.158	0.147	8.1	7.0
5	0.057	0.054	13.5	5.26
7	0.029	0.028	18.9	3.45

Table 5-2 - Measured and computed peaks in grossly slope overloading condition.

5-5 - Frequency response

The experimentally evaluated frequency response, of the MC-3417 (3-bit shift register) system of figure 5-1, is shown in figure 5-25. Figure 5-26 shows similar data for the MC-3418 device (4-bit shift register). The sampling rate was 16.0 KHZ for both tests. Experimental data for the MC-3417 and the MC-3418 devices are given in tables 5-3 and 5-4, respectively. The transfer function characteristics shown in figures 5-25 and 5-26, indicate a very large attenuation near the cut-off frequencies (approximate rate of -360 DB/decade). This fast drop in the transfer characteristics can

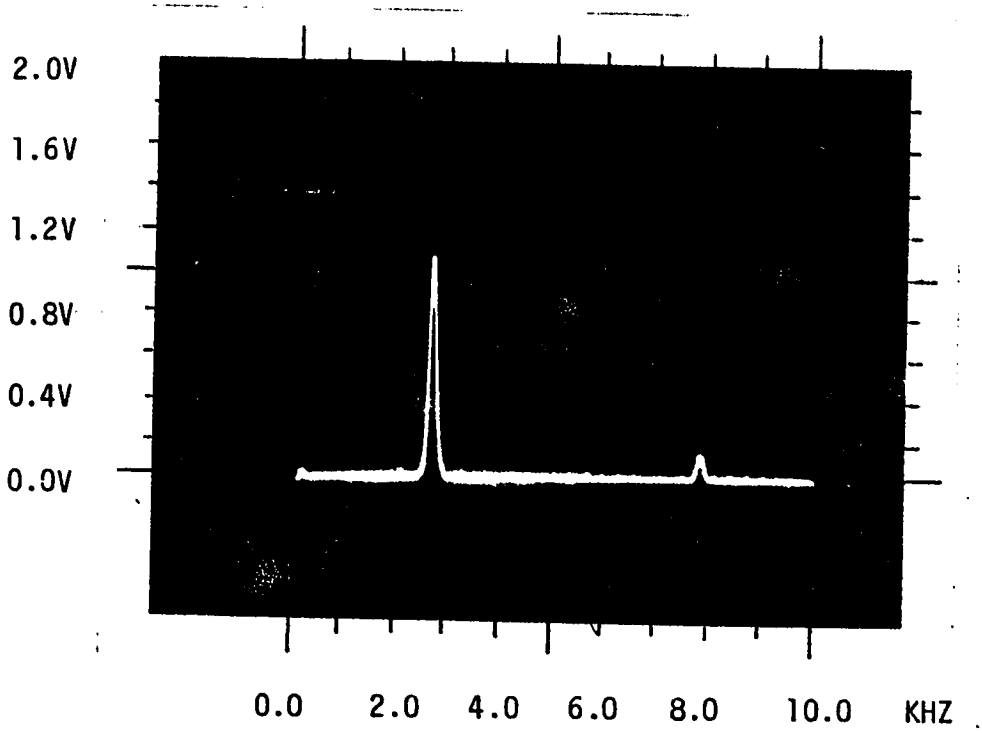


Fig.5-23 - Frequency spectrum of the decoded wave at grossly slope overloading condition. The third harmonic is also seen in this figure.

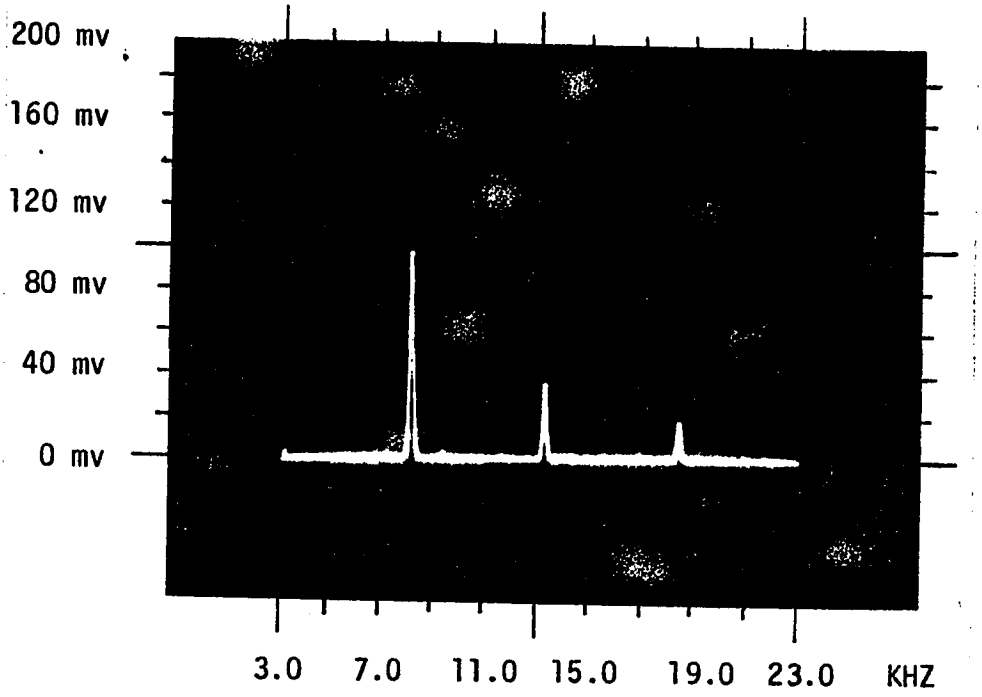


Fig.5-24 - Frequency spectrum of the triangular decoded wave showing 3rd, 5th and 7th harmonics of the fundamental.

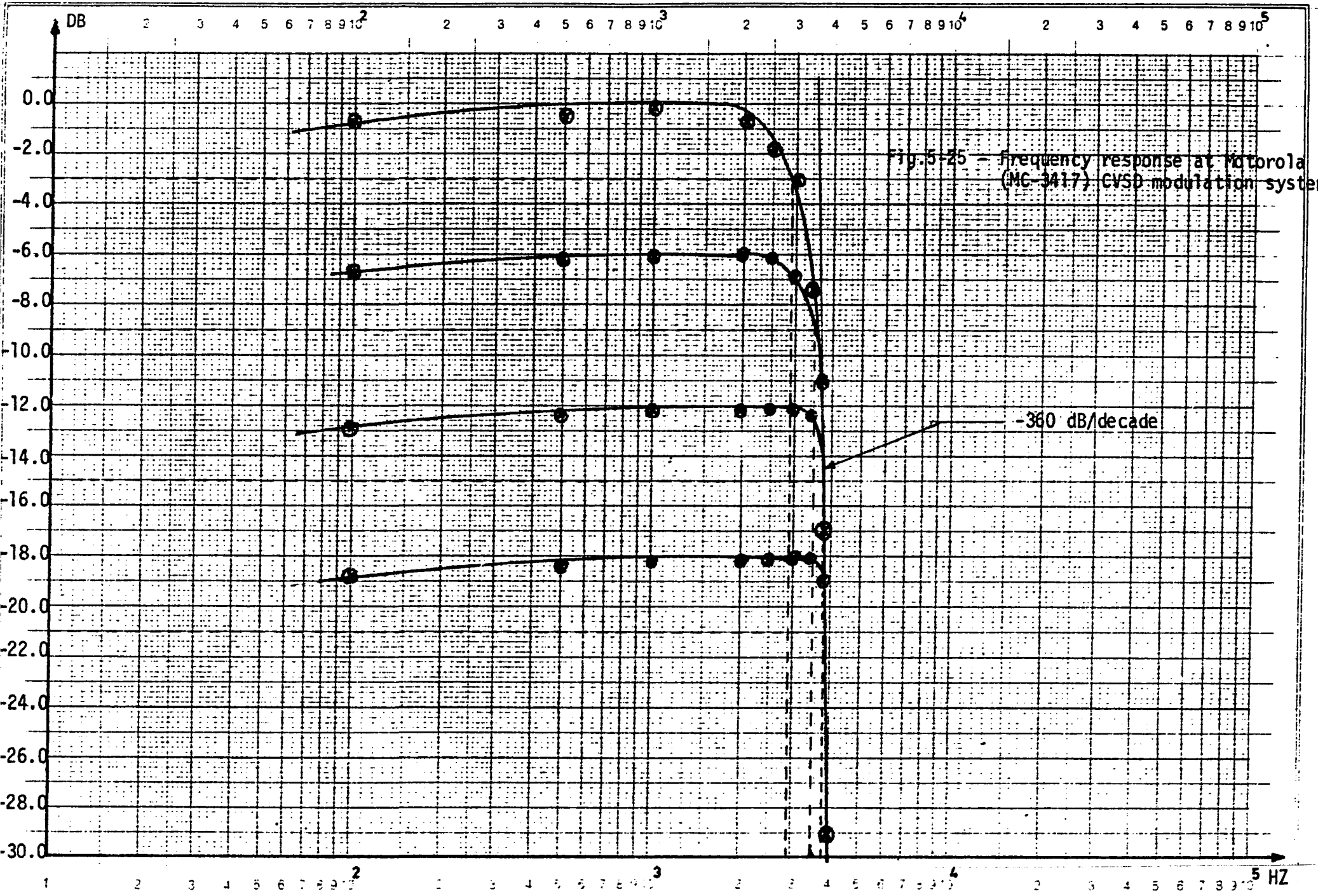


Fig.5-25 – Frequency response at Motorola (MC-3417) CVSD modulation system.

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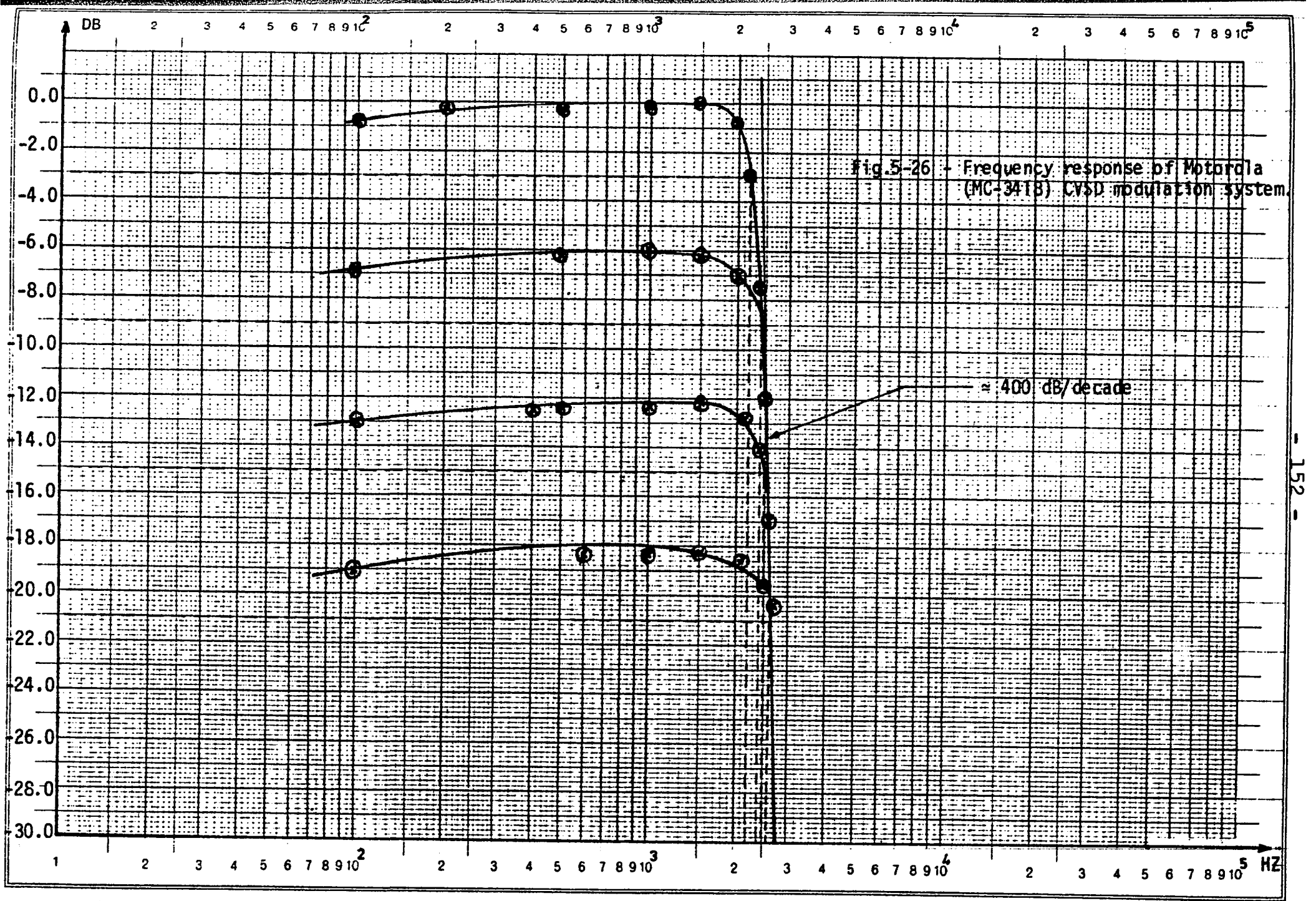

Fig.5-26 - Frequency response of Motorola (MC-3418) CVSD modulation system.

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Input condition peak value	2.0V 0.0 DB		1.0V -6.0 DB		500 mv -12.0 DB		250 mv -18.0 DB	
Output peak value* at f_s	Volt	DB	Volt	DB	Volt	DB	Volt	DB
100	1.84	-0.7	0.92	-6.75	0.46	-12.77	0.23	-18.93
500	1.9	-0.4	0.98	-6.2	0.48	-12.4	0.235	-18.6
1000	1.98	-0.09	0.99	-6.1	0.49	-12.2	0.24	-18.42
2000	1.84	-0.7	0.99	-6.1	0.495	-12.13	0.245	-19.24
2500	1.63	-1.8	0.995	-6.06	0.495	-12.13	0.245	-19.24
3000	1.41	-3.0	0.92	-6.75	0.490	-12.2	0.245	-19.24
3200	1.13	-4.95	0.92	-6.75	0.49	-12.2	0.245	-19.24
3400	0.85	-7.45	0.71	-9.0	0.49	-12.2	0.245	-19.24
3600	0.57	-11.0	0.5	-12.1	0.45	-12.9	0.240	-19.42
3800	0.28	-17.0	0.28	-17.0	0.28	-17.0	0.20	-20.1
4000	0.07	-29.0	0.07	-29.0	0.07	-29.0	0.07	-29.0

* The fundamental of the triangular decoded wave was considered as the pure decoded wave.

Table 5-3 - Frequency response data for the MC-3417 device.

Input condition peak value	2.0V 0.0 DB		1.0V -6.0 DB		500 mv -12.0 DB		250 mv -18.0 DB	
Output peak* value at f_s	Volt	DB	Volt	DB	Volt	DB	Volt	DB
100	1.84	-0.7	0.92	-6.8	0.46	-12.9	0.23	-18.93
500	1.90	-0.4	0.98	-6.2	0.47	-12.6	0.235	-18.6
1000	1.95	-0.2	0.99	-6.1	0.48	-12.4	0.24	-18.4
1500	1.98	-0.09	0.92	-6.75	0.49	-12.2	0.245	-18.24
2000	1.84	-0.7	0.9	-6.94	0.46	-12.9	0.235	-18.6
2100	1.7	-1.43	0.85	-7.45	0.41	-13.76	0.23	-18.93
2200	1.41	-3.0	0.8	-7.96	0.40	-13.98	0.212	-19.5
2400	0.85	-7.45	0.78	-8.2	0.4	-13.98	0.212	-19.5
2500	0.56	-11.0	0.54	-11.4	0.4	-13.98	0.212	-19.5
2600	0.283	-17.0	0.28	-17.0	0.28	-17.0	0.198	-20.1
2800	0.025	-38.0	0.025	-38.0	0.025	-38.1	0.025	-38.1
3000	0.02	-39.5	0.02	-39.5	0.02	-39.5	0.02	-39.5

* The fundamental of the triangular decoded wave was considered as the pure decoded signal.

Table 5-4 - Frequency response data for the MC-3418 device.

be explained theoretically by utilizing the description of the system for the grossly slope overloaded condition.

Again consider figure 5-11. When grossly slope overloaded, the syllabic voltage V_{cs}, across the capacitor C_s charges and discharges as before. The system is able to track the higher frequencies as long the capacitor C_s is able to charge to sufficiently high average d.c. values; i.e. the charging period T_2 in figure 5-11 is larger than the discharging duration T_1. The effect of charging and discharging is to increase the d.c. across C_s. At a certain input frequency f_s providing grossly slope overloading condition, the total duration of the "1" or of the "0" state is T, where $T = \frac{1}{2f_s}$. The coincidence output $\overline{G(t)}$ can be represented in time as follow:

$$\overline{G(t)} = \begin{cases} 1 \text{ ; (discharging region)} & 0 \leq t \leq T_1 \\ 0 \text{ ; (charging region)} & T_1 \leq t \leq T_2 \end{cases}$$

Where: $T_1 = (n-1)T_p$

$$T_2 = T - T_1 = [N - (n-1)]T_p \qquad (5\text{-}16)$$

n is the shift register length and N of is the number of consecutive "1's"or "0's"in half period of the input as determined by the ratio $f_p/2f_s$. For one cycle of the input signal, the coincidence output is repeated two times, once for the "1" state and once for the "0" state of L(t). The syllabic capacitor C_s charges

during the "0" state of $\overline{G(t)}$ and discharges during the "1" state of $\overline{G(t)}$ (see section 5-3). By choosing a new input frequency f_{s2}, such that $f_s' > f_s$, the charging period, T_2 at f_s' is now smaller than at f_s. Since n is a fixed number, the discharging period T_1 is not affected with the change of the input frequency. By further increasing the input frequency f_s a condition may be reached where the charging period is equal to the discharging period; i.e. $T_1 = T_2 = (n-1)T_p$ or $T = 2(n-1)T_p$. The frequency f_s at which this condition may occur is:

$$f_s^* = \frac{1}{2T} = \frac{1}{4(n-1)T_p}$$

OR:

$$f_s^* = \frac{f_p}{4(n-1)} \qquad (5\text{-}17)$$

For any frequency above f_s^* the charging period is smaller than the discharging period. Consequently capacitor C_s will experience a decline in its average voltage. The loop gain of the system (determined by the ratio of V_{cs}/R_x) is thereby decreased and the peak-to-peak amplitude of the decoded signal is smaller. Assuming a symmetrical digital pattern L(t) above f_s^*, the charging period T_2 will continue decreasing until a frequency f_s is reached where $T_2 = \frac{1}{2} T_1$; i.e. $T = \frac{3}{2} T_1 = \frac{3}{2}(n-1)T_p$. This frequency f_s^{**} is given by:

$$f_s^{**} = \frac{1}{2T} = \frac{1}{3(n-1)T_p}$$

OR:

$$f_s^{**} = \frac{f_p}{3(n-1)} \qquad (5\text{-}18)$$

Again assuming symmetrical digital pattern L(t) above f_s^{**}, the charging period T_2 can further decrease until T_2 completely vanishes; i.e. T_2=0. At this condition $T = T_1 = (n-1)T_p$ and C_s is at its minimum voltage V_{csmin}, as determined by equation 5-13. The frequency f_s^{***} at which $T_2 = 0$ is given by:

$$f_s^{***} = \frac{1}{2T} = \frac{1}{2(n-1)T_p}$$

OR:

$$f_s^{***} = \frac{f_p}{2(n-1)} \qquad (5\text{-}19)$$

The above analysis indicates that the loop gain of the Motorola device will begin decreasing at the condition given by equation 5-17. The rate of decline is small at the beginning, since the charging period T_2 is still much larger than T_1. At the condition given by equation 5-18 and above the roll-off is much faster, since now the discharging period is comparable to the charging period. When T_2 becomes inappreciable the roll-off again becomes gradual, but with extremely small loop gain. Equation 5-19 indicates the frequency of no further roll-off and a gain equal to that of the idle condition.

The theoretical critical frequencies f_s^*, f_s^{**} and f_s^{***} for the MC-3417 and MC-3418 devices are given in table 5-5. The corresponding experimental frequencies of figures 5-25 and 5-26 are also given in table 5-5. The table indicates that, the experimental data corroborates the theoretical values at f_s^* and f_s^{***}. Exact estimation of f_s^{**} from the experimental is not possible unless

the level of the decoded signal is defined at this frequency. An approximate value of f_s^{**} is given in table 5-5.

The cut-off frequencies for the CVSD modulation system using either MC-3417 or MC-3418 at different amplitudes of the input signal are tabulated in table 5-6. At a fixed sampling rate, the MC-3418 device exhibits low bandwidth. This is due to the difference in the number of shift registers used to detect the slope of the input signal. Companding with a larger number of shift registers is slower to respond for any momentary variation in the slope of the input signal, than a system with a small number of shift registers.

Critical frequency	Condition	MC-3417 n = 3		MC-3418 n = 4		Units
		Theoretical	Experimental	Theoretical	Experimental	
f_s^*	$T_2 = T_1$ (eq.5-17)	2.0	1.9	1.33	1.4	KHZ
f_s^{**}	$T_2 = \frac{1}{2}T_1$ (eq.5-18)	2.67	≈2.95	1.78	≈1.9	KHZ
f_s^{***}	$T_2 \simeq o$ (eq.5-19)	4.0	4.05	2.67	2.8	KHZ

Table 5-5 - Theoretical and experimental critical frequencies for the Motorola devices (MC-3417 and MC-3418).

Input signal DB	Cut-off frequencies		Unit
	MC-3417	MC-3418	
0.0	2.85	2.25	KHZ
-6.0	3.30	2.45	KHZ
-12.0	3.40	2.50	KHZ
-18.0	3.45	2.70	KHZ

Sampling rate f_p = 16.0 KHZ

0.0 DB = 4.0 V_{p-p}

Table 5-6 - Bandwidths of a (CVSD) system at different amplitudes of the input signal.

CHAPTER - 6

TEST RESULTS OF A DIGITALLY CONTROLLED COMPANDED DELTA MODULATOR

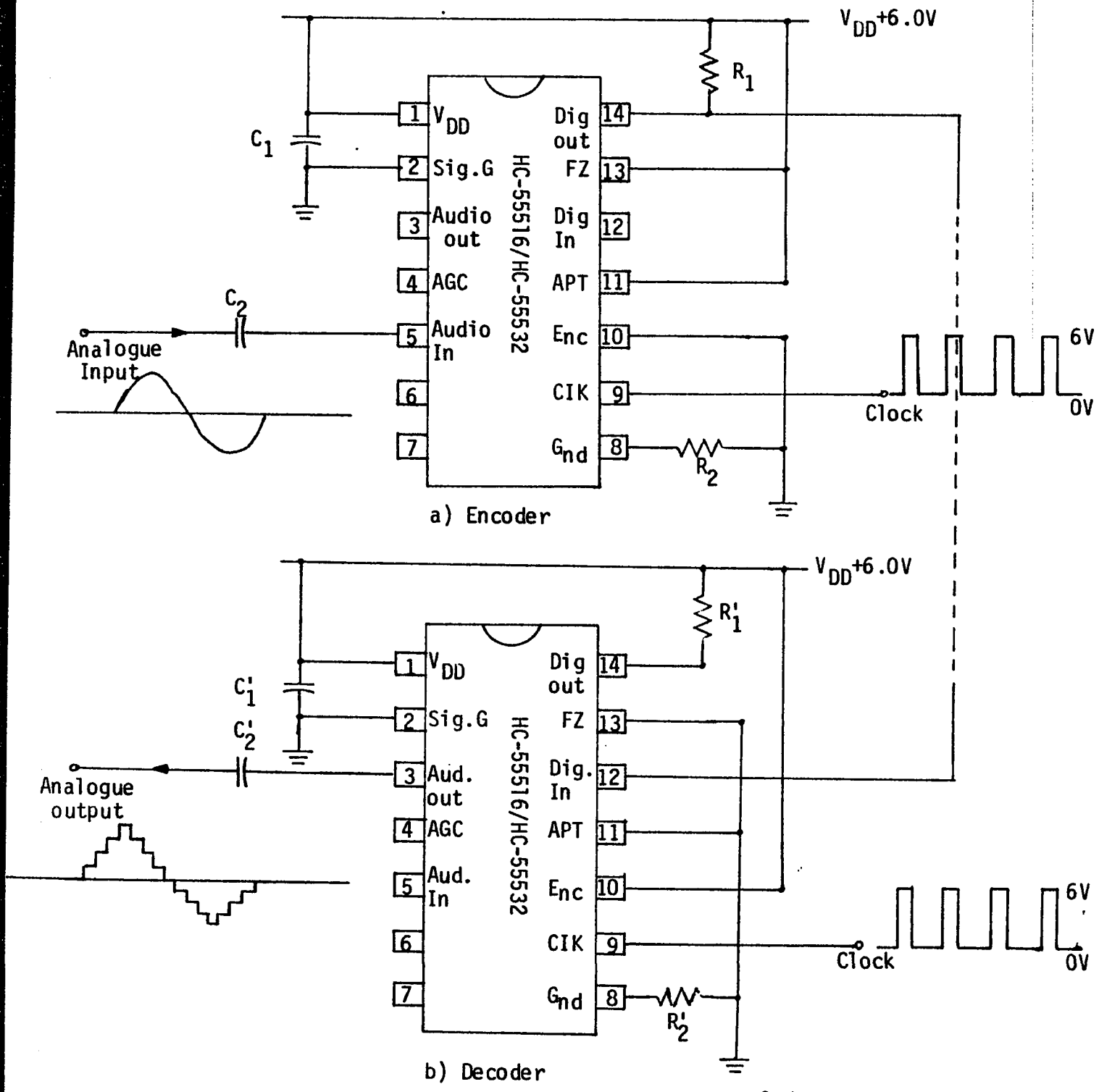
6-1 - Introduction

The continuous variable slope delta (CVSD) modulation system, built as an integrated circuit by Harris Semiconductors Corporation (HC-55516/HC-55532), was also tested for its operation. It is a syllabically companded system, for which companding is entirely digitally accomplished. As a single IC is sufficient only for half duplex operation (encoder/decoder), two chips of HC-55516 were used to construct a complete system consisting of an encoder and a decoder. A recommended evaluation hook-up for optimizing the performance of the Harris device is shown in figure 6-1 |26|. The resulting system was tested in similar way to the preceding; i.e. for idling condition, normal operation, and slope overloading condition.

The general behaviour of the Harris device is also discussed on the base of it's parallel analogue equivalent system.

6-2 - Idling condition

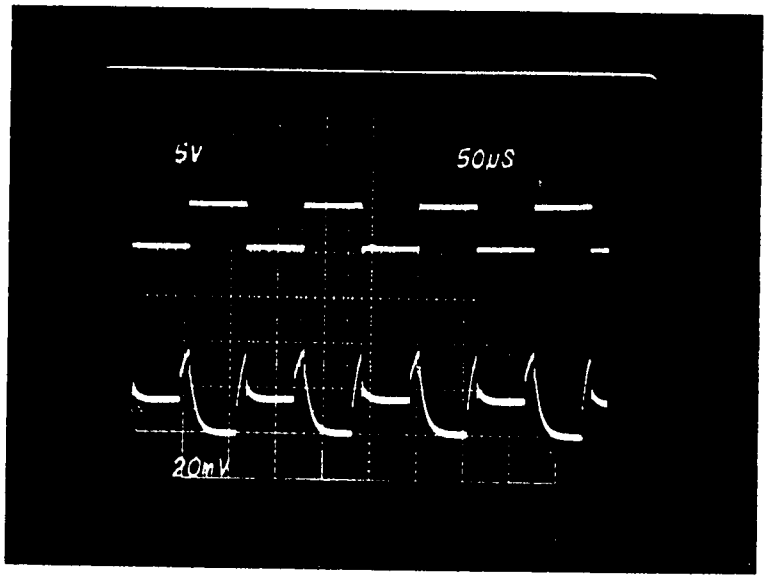
The encoder shown in figure 6-1a is usually set for idling operation either by making the analogue input zero volt or by putting the "Force zero (FZ)" pin low (ground) by an external input. The idling pattern at the output of the encoder consists of alternate binary levels of one's and zero's, at a frequency equal to half the sampling rate f_p (figure 6-2a). The output of the decoding network is shown more vividly in figure 6-3b. For theoretical



Codec Components

R_1 , R'_1	4.7KΩ
R_2 , R'_2	10Ω
C_1,C'_1,C_2	0.1 µF
C'_2 ,	0.47 µF

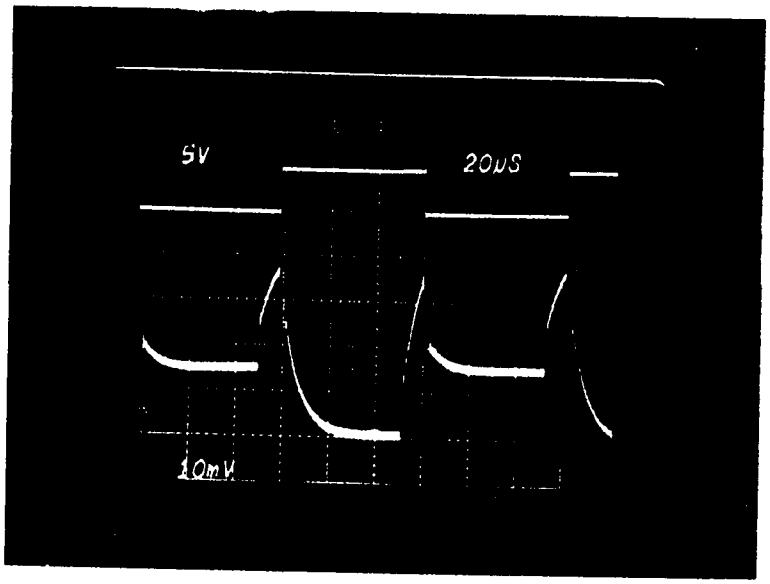
Fig. 6-1 - CVSD modulation system using Harris devices HC-55516/HC-55532.



a) Digital pattern at the the encoder output.

b) Waveform at the decoder output.

Fig.6-2 - Idle condition pattern of the Harris (HC-55516) CVSD system.

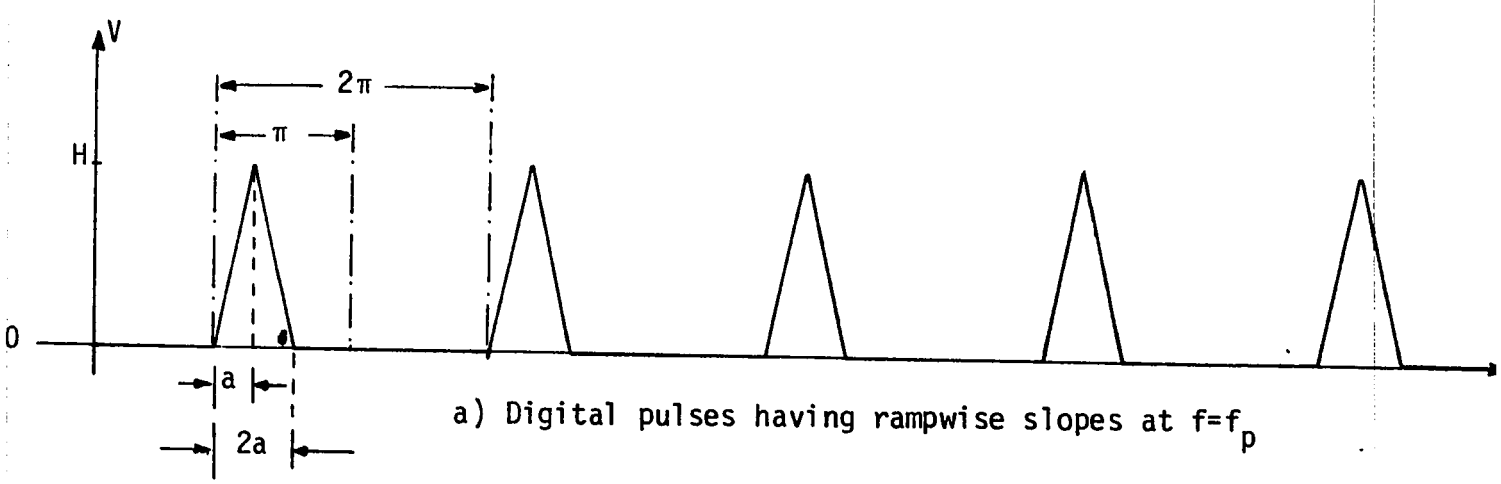


a) Digital pattern.

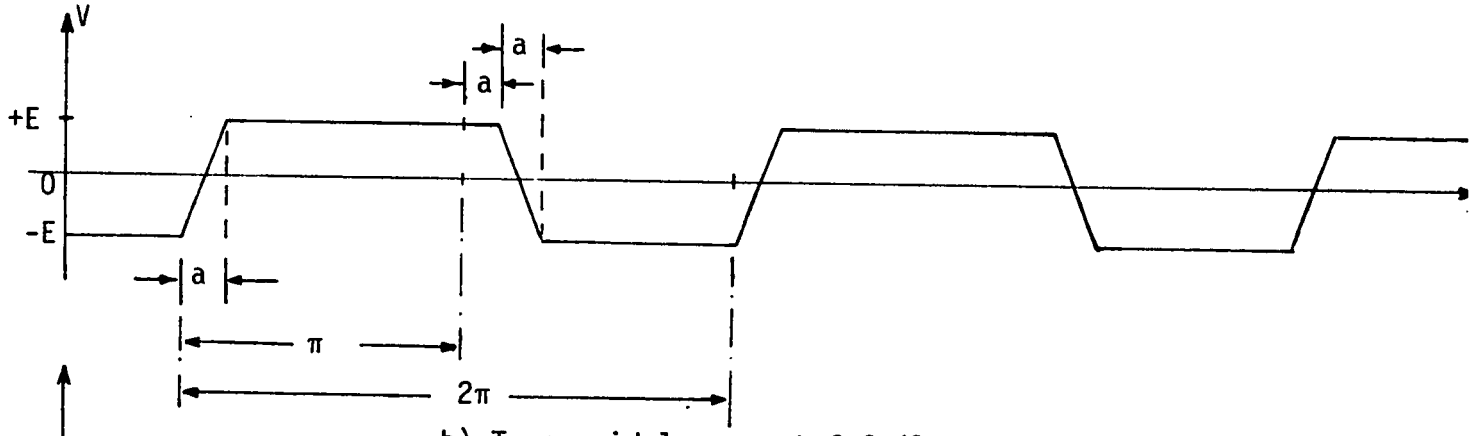
b) Decoded waveform.

Fig. 6-3 - Idling pattern in more detail.

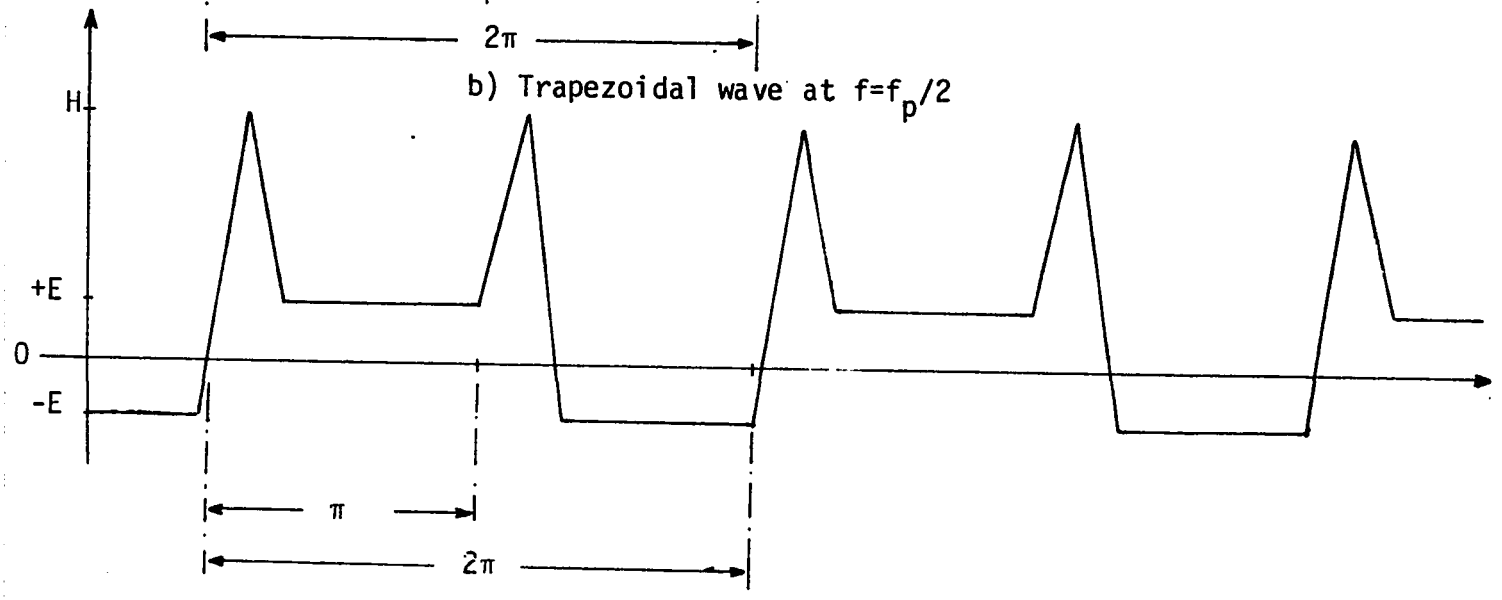
analyses, this waveform can be considered to be composed of the sum of a train of positive pulses with a ramp-wise rising and falling edges at a frequency equalling the sampling rate f_p (figure 6-4a) and of a trapezoidal wave at a frequency equal to half the sampling rate $f_p/2$ (figure 6-4b). This trapezoidal wave contains assymetry in its periodicity; i.e. the time durations of the positive and the negative constant levels are not equal. The addition of these two signals (figure 6-4c) results in approximate sketch of the actual decoded waveform. The frequency spectrum of the decoded signal at idling shows two groups of peaks (figure 6-5). The first group occurs at $f_p/2$ and its odd multiples. The second group occurs at f_p and its consecutive multiples. These peaks are interpreted by the Fourier series expansion of the two assumed waveforms. Figure 6-6a and figure 6-6b shows the approximated computed peaks in polar form (C_n) at discrete frequencies. These peaks results from the Fourier series expansion of the trapezoidal wave (appendix 4-2.2) and of the ramp-wise pulses (appendix 4-3), respectively. Phasor addition of these two group peaks gives the total theoretically expected spectrum of the approximated sketch of the decoded wave (figure 6-6c). In figure 6-6c, peaks at $f_p/2$ (8.0 KHZ) and its odd multiples results only from the odd harmonics of the trapezoidal waveform. The peaks at f_p (16.0 KHZ) and its consecutive multiples results from the phasor addition of the even harmonics of the trapezoidal waveform and of the harmonics of the ramp-wise pulses. The computation of these peaks is given in appendix 4-4.2. The difference between the computed



a) Digital pulses having rampwise slopes at $f=f_p$



b) Trapezoidal wave at $f=f_p/2$



c) Approximate waveform of a+b.

Fig. 6-4 - Approximate waveform of the idle condition pattern of Harris CVSD system using superposition.

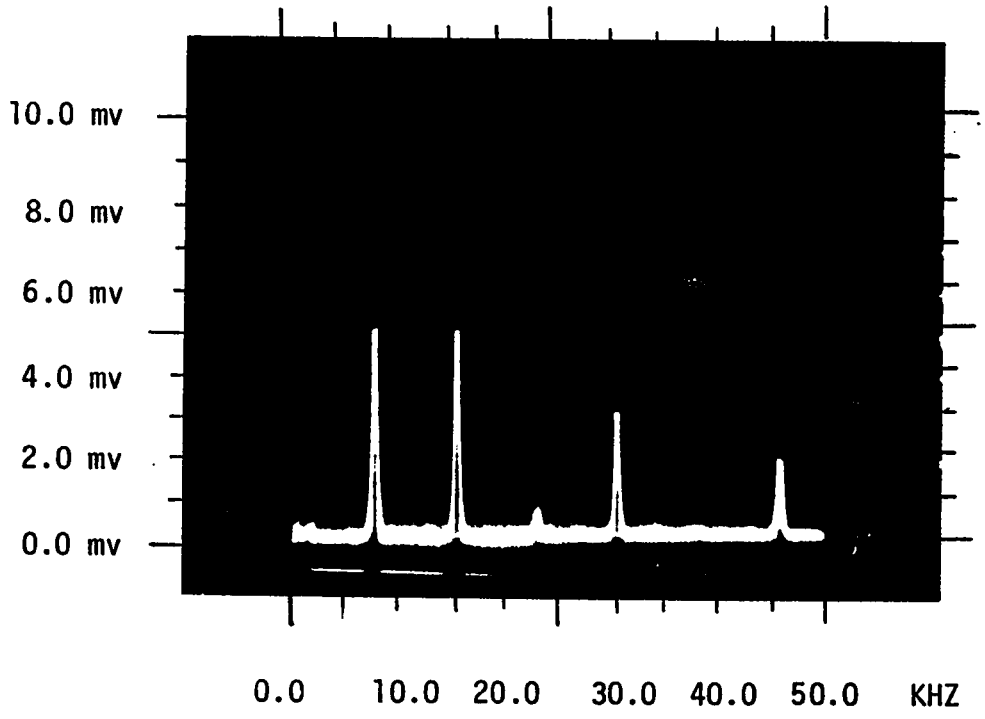


Fig. 6-5 - Frequency spectrum of the decoded wave under idling condition.

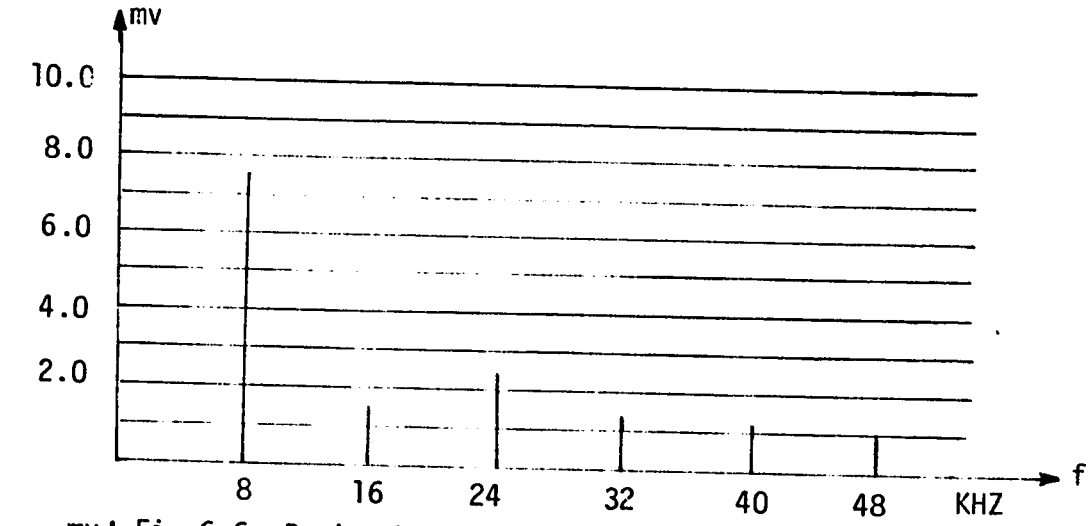


Fig.6-6a-Peaks due to the trapezoidal wave

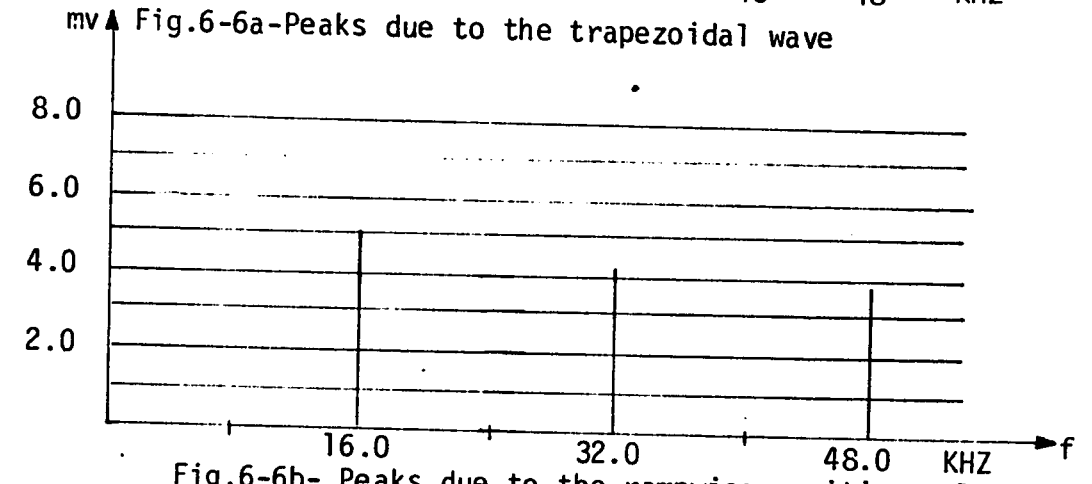


Fig.6-6b- Peaks due to the rampwise positive pulses.

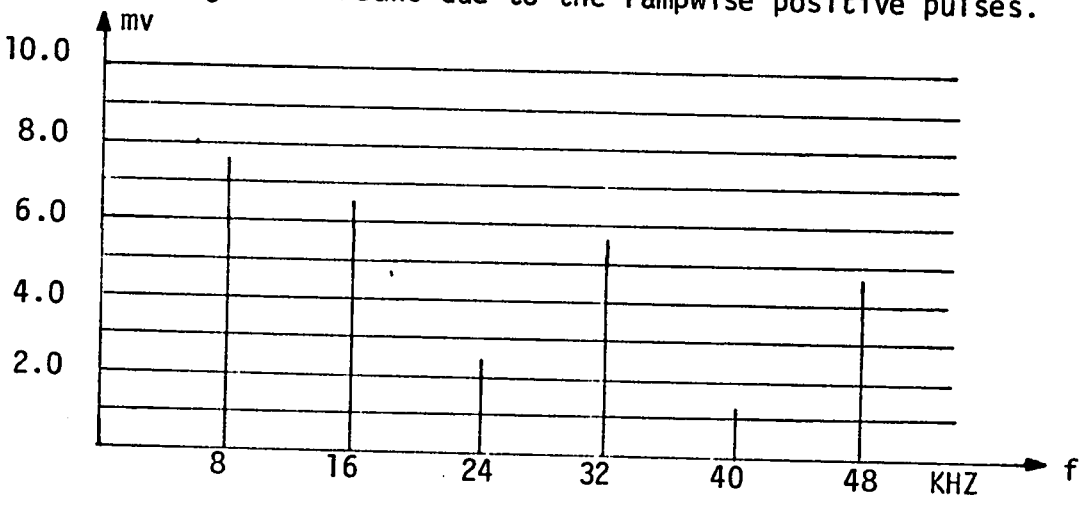


Fig.6-6c- Theoretically expected spectrum of the idle condition pattern (Phasor addition of a and b).

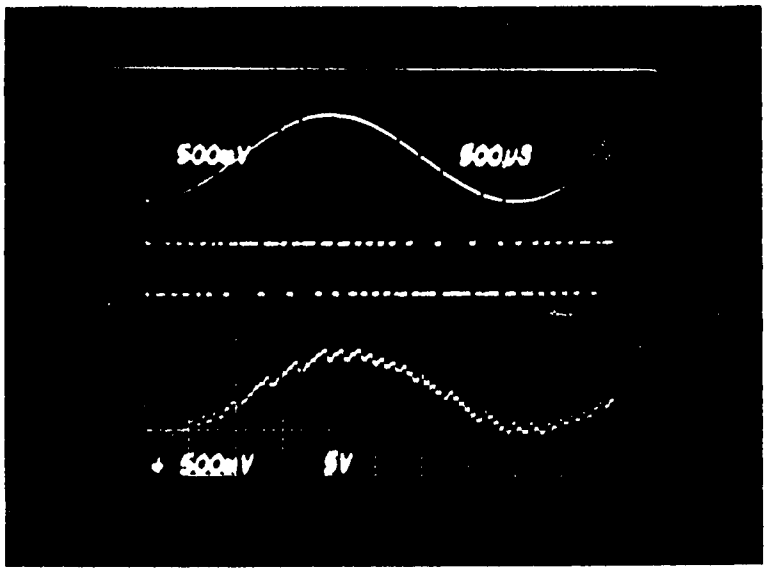
and the measured peaks in table 6-1, can be interpreted by the probable error between the approximated sketch and the actual wave of the decoded signal. In sketching the decoded wave, it was assumed that the trapezoidal wave has an equal rising and falling period (a), also it was assumed that the delaying period of the falling edge from π radians is also equal to the period (a) seconds. A similar assumption (equal rising and falling time periods) was considered for the ramp-wise pulses. In general, the actual frequency spectrum of the decoded wave (figure 6-5) is in consistence with that theoretically expected (figure 6-6c).

Peak No	Computed peak mv	Frequency KHZ	Measured peak mv	% difference w.r.t. the computed peak
1st	7.507	8.0	7.07	5.8
2nd	6.431	16.0	6.788	5.6
3rd	2.325	24.0	1.13	51.4
4th	5.628	32.0	4.24	24.7
5th	1.133	40.0	0.43	62.0
6th	4.717	48.0	2.546	46.0

Table 6-1 - Computed and measured peaks at idling condition.

6-3 - Normal operation

In the normal operating condition, the continuously variable slope delta (CVSD) modulator, adapts its feedback signal according to the continuous slope variation of the input signal. This adaptation rule enables the system to track a wider range of input signal (wider range of amplitudes at a fixed frequency or a wider range of frequencies at a fixed amplitude). In the Harris device, the adaptive network is completely digital. The digitally controlled signal is converted to a multilevel quantized feedback signal. The behaviour of the system shown in figure 6-1, with a sinusoidal input and in normal operating condition is shown in figure 6-7. The frequency spectrum of the decoded wave (figure 6-7c) shows two peaks of 425 mv at $\pm$ 250 HZ and relatively low amplitudes of noise (figure 6-8). The peak of the decoded wave is smaller than the amplitude of the input signal (500 mv) due to the filtering of the stepwise decoded waveform by the spectrum analyzer. Figure 6-9 shows this noise more vividly with an average peak value of 10 mv. First overtone component of the fundamental at 16.25 KHZ is also visible in figure 6-9. Experimentally it was corroborated that, the overall distribution of this noise is a function of the sampling rate (see chapter three section 3-4.3). By applying a similar interpretation as that for the LDM system, this noise is referred to as the quantization noise. Overtone components of the fundamental and its noise translated by the sampling rate and its multiples are shown in figure 6-10.



a) Sinusoidal analogue input.

b) Digital output.

c) Decoded output.

Fig. 6-7 - Normal operating condition waveforms of the Harris CVSD system.

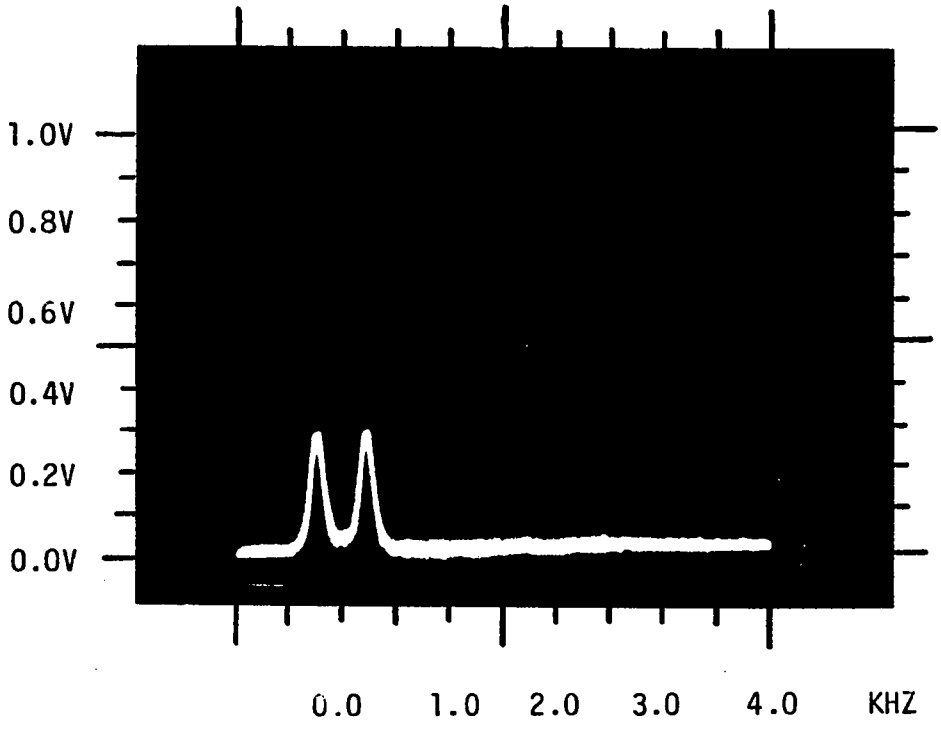


Fig. 6-8 - Frequency spectrum of the decoded wave under normal operating condition.

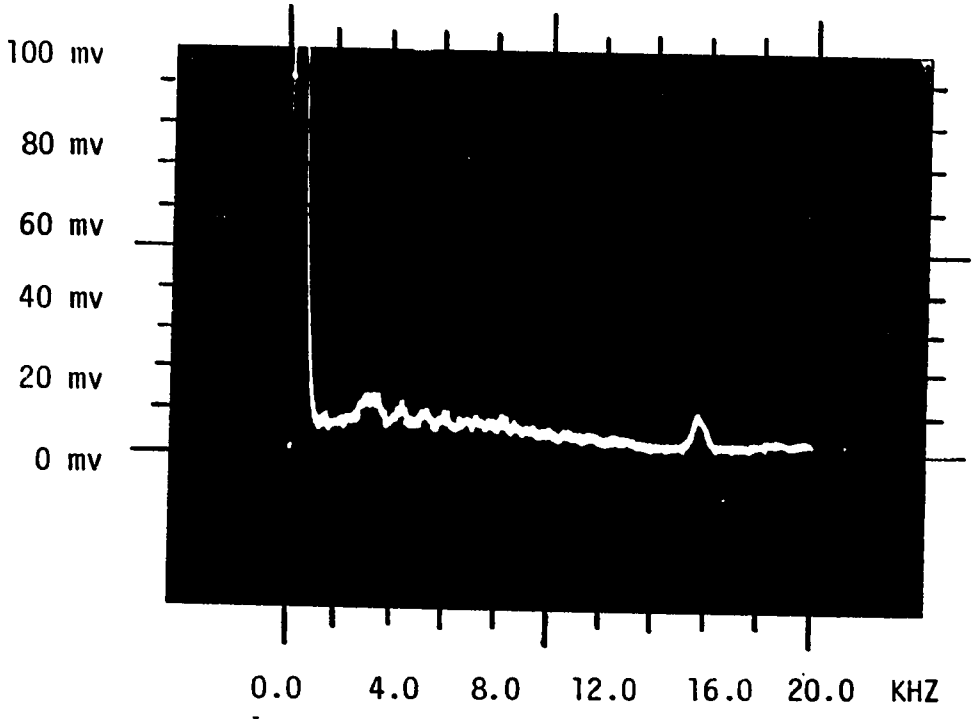


Fig. 6-9 - Accompanied noise with the fundamental of the decoded wave. First overtone component also appears at 16.25 KHZ.

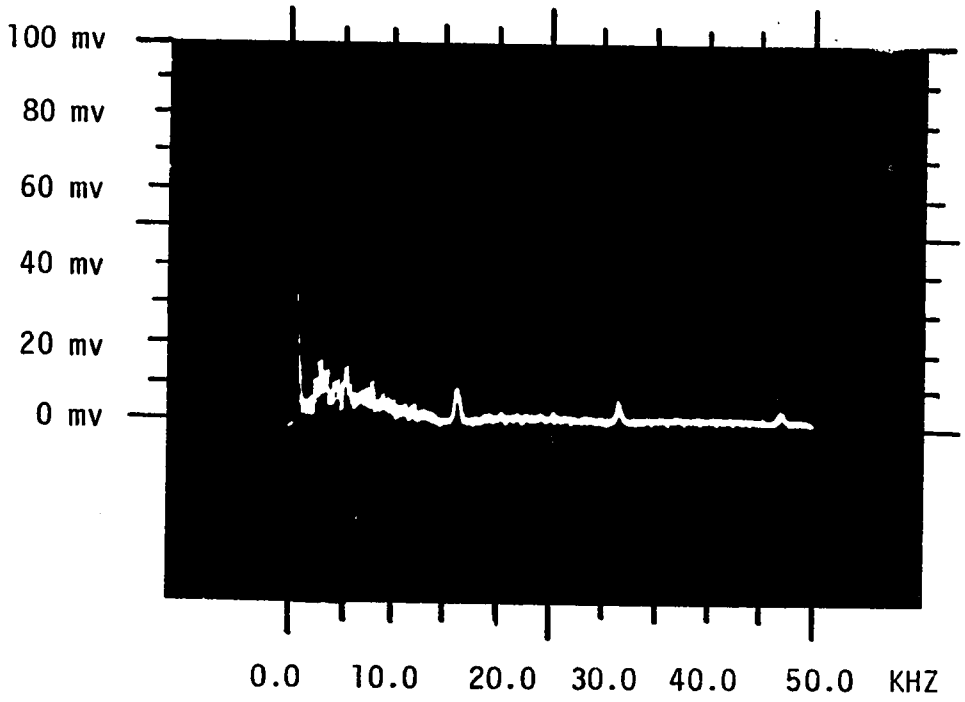


Fig. 6-10 - Overtone components at the consecutive multiples of sampling rate f_p.

The argument for these components is same as that given in chapter three. The amplitudes of these components together with their relative amplitudes are tabulated in table 6-2. A low-pass filter at the output of the decoder will pass only those frequencies which are below its cut-off frequency f_c. The noise at frequencies higher than f_c (part of quantization noise and the overtone components) will be attenuated considerably.

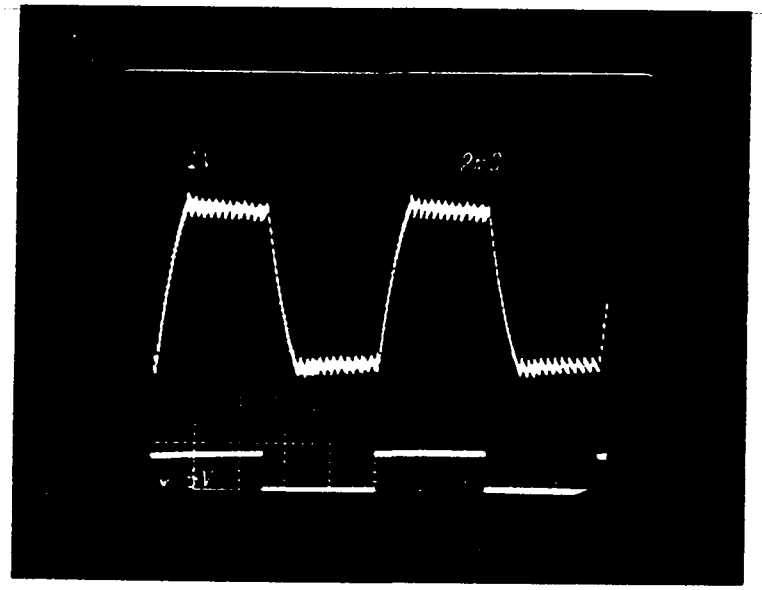
Overtone peak No.	Frequency KHZ	Amplitude peak value mv	% amplitude w.r.t. the fundamental
1st	16.0 $\pm$ 0.25	13.0	3.0
2nd	32.0 $\pm$ 0.25	7.0	1.7
3rd	48.0 $\pm$ 0.25	4.25	1.0

Fundamental peak of 425 mv at 250 HZ

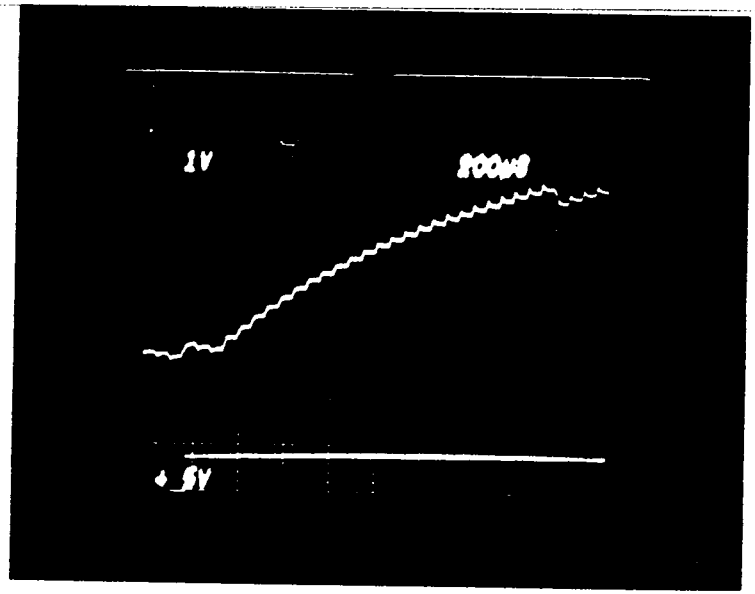
Table 6-2 - Amplitudes of overtone components in normal operating condition.

6-4 - Step response

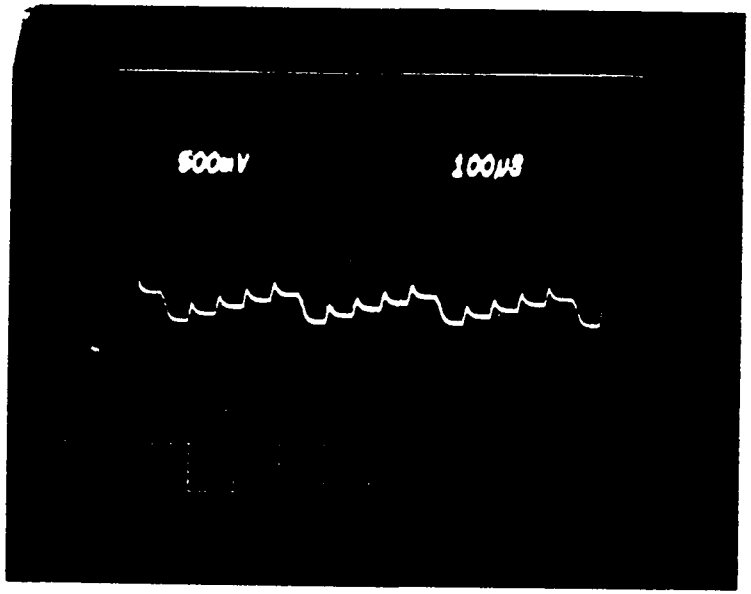
The step response of the Harris (CVSD) modulation system is shown in figure 6-11a. A low frequency square wave was applied to achieve the response. The decoded signal rises/falls in steps depending upon the newly switched level of the input step (figures 6-11b and 6-11c). At the flat portion the decoded signal oscillates (hunts) about the constant level (figure 6-11d). The decoded signal needs a measurable time to assume the idling condition. This time depends upon the level and the frequency of the input signal. Both the rising and the falling portions are essentially identical. Its nonlinear waveshape (approximately exponential) is due to variation of the step size at the successive sampling instants. The visual impression is that, companding starts with a larger step and then decreases gradually at the successive sampling periods until the hunting portion is reached. To verify this visual observation and to define the relation by which the step size changes, analysis of the analogue circuit shown in figure 6-12,which parallels the function of the Harris device |11 |, will be made. The logic at the output of the shift registers in figure 6-12 was also modified, since the published logic (exclusive NOR gate in |11| and exclusive OR gate in |26|) does not operate properly. It does not provide the "1" state whenever there are either three or more consecutive "1's" or "0's"in the L(t) pattern. This type of function is necessary if the system is to operate as described in reference |11|. Also an



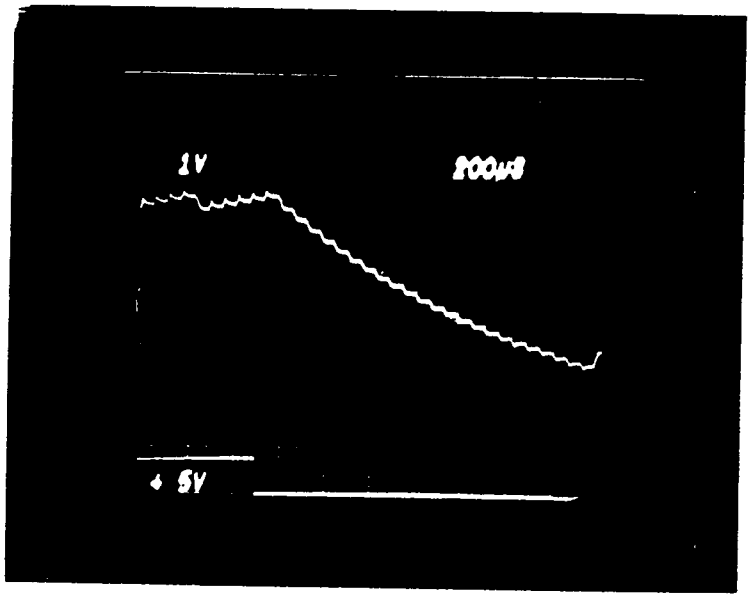
(a)



(b)



(d)



(c)

Fig. 6-11 - Step response of the Harris (HC-55516) CVSD modulation system.

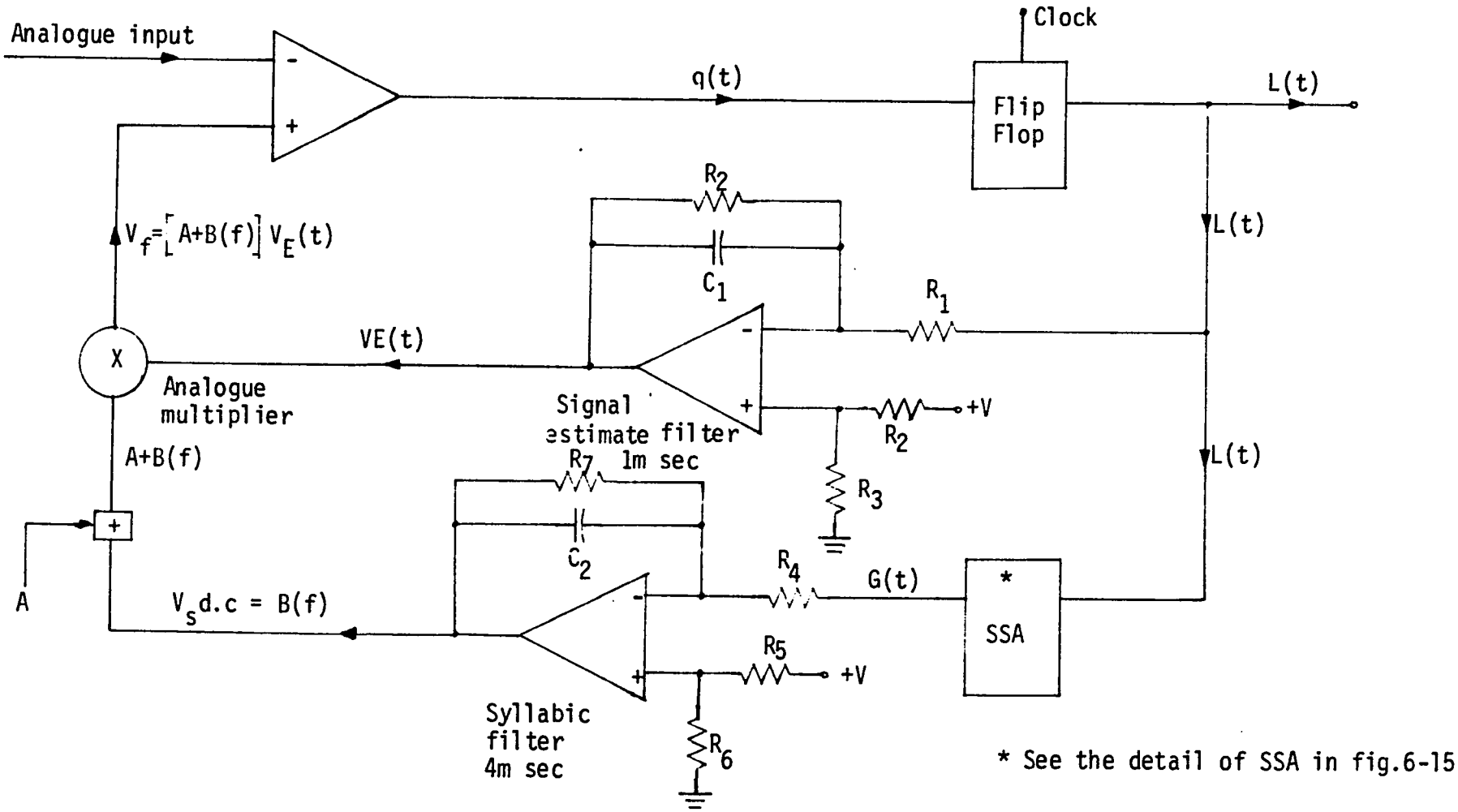


Fig. 6-12 - An analogue CVSD modulation system which parallels the function of Harris device.

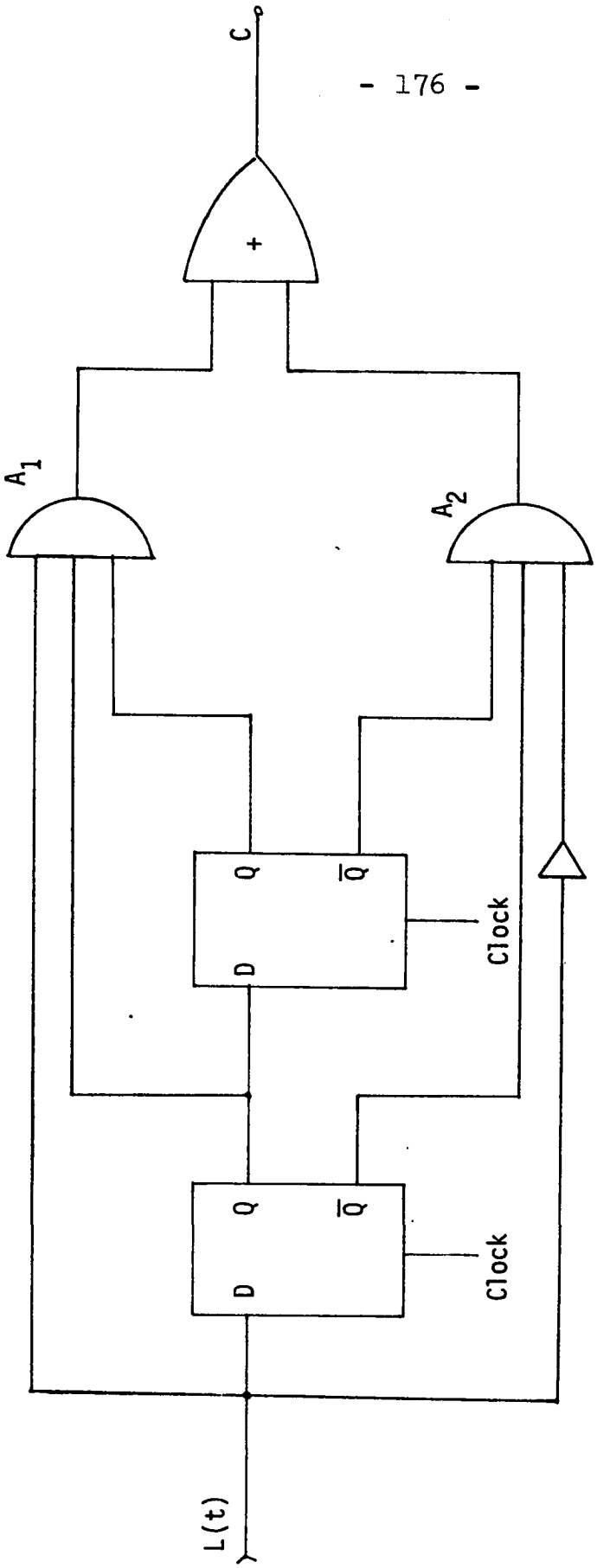


Fig. 6-13 - Schematic detail of the modified SSA algorithm. Output (c) has the "1" state whenever there are three consecutive "1's" or three "0's" in the L(t) pattern.

adder circuit was included in the schematic so that the addition of a constant d.c. level (A) and of the d.c. component resulting at the output of the syllabic filter are fed to the multiplier.

Again, this alteration is necessary for concurrence of operation and the schematic. Under the normal operating condition, and with a low sinusoidal frequency, the signal estimate filter in the first feedback loop is able to track the input without experiencing any slope overloading. For this condition, there are an inadequate number of consecutive "1's"or "0's"in L(t) pattern for companding. Consequently the syllabic filter output is at its minimum level (probably zero volt). As the slope of the input is increased by changing the frequency of the input signal, the signal estimate filter fails to track these frequencies and starts experiencing some slope overloading. The consecutive "1's"and "0's"start appearing in the L(t) pattern and the logic value, at the SSA output, will assume the "1" state for certain time durations. This state causes the syllabic capacitor to charge. It discharges during the "0" state. The effect of charging and discharging the capacitor is to raise the slowly varying voltage (V_s) at the low-pass syllabic filter output. The V_s signal controls the gain of the multiplier. Because of the low-pass filter and a zero minimum, V_s is nearly a constant value at a fixed input amplitude and frequency. Hence, it be referred to as a d.c. signal.

The function of the second feedback loop is to aid the signal estimate filter to track wider range of frequencies or amplitudes. The magnitude of V_s is a monotonically increasing function of f_s, as long as the system is not completely slope overloaded. This is because as f_s increases, more consecutive "1's"and "0's"are present in L(t). Therefore, the charging period (T_{ch}) is longer, whereas the discharging period (T_{disch}) is a constant for a fixed shift register length; i.e. $T(disch)_{min} = nT_p$, where n is the shift register length and T_p is the sampling period. The V_s d.c. component reaches its maximum value at a frequency f_{s_o} where the system has just begun to be completely slope overloaded. At this situation the charging period is at its maximum value; i.e. $T(ch) = T_o - T(disch)$, where $T_o = \frac{f_{so}}{2}$ is the total period of either the "1" or the "0" state of L(t). At frequencies above f_{s_o} the d.c. component (V_s d.c.) will decrease monotonically with f_s. This is because, if $f_{s_1} > f_{s_o}$, $T_1 < T_o$ and since T(disch) remains constant, then T_1 (ch) < T_o(ch). The rate of decrease of the d.c. signal (V_s d.c) depends on f_s (will be determined later in section 6-5) upto a frequency where T(ch) = 0; i.e. when the total period of the "1" or of the "0" state is equal to or less than T(disch); i.e. $T = nT_p$.

The feedback signal $V_f(t)$ under any operating condition at the output of the multiplier can be written as:

$$V_f(t) = \left[A + B(f_s) \right] V_E(t) \qquad (6\text{-}1)$$

where: A is an external d.c. component.

$B(f_s)$ is the d.c. component (V_s d.c) resulting at the output of the syllabic filter and dependent of the signal frequency f_s.

$V_E(t)$ is the signal at the output of the signal estimate filter. It is approximately the integral of the digital pattern L(t).

Further discussion regarding the $V_E(t)$ and $B(f_s)$ terms is postponed after examining the behaviour of the system under slope overloading condition.

6-5 - Slope overloading condition

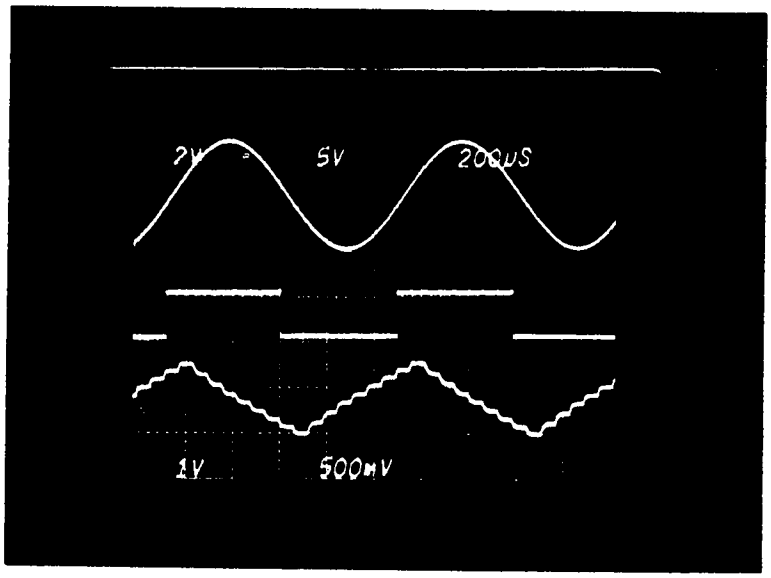
By increasing the amplitude E_s or the frequency f_s of the input signal, a condition may be reached where the CVSD system is slope overloaded. The digital pattern of the output of the Harris device encoder for excessive slope overloading is a rectangular wave at a frequency equal to that of the input signal f_s and a peak-to-peak amplitude given by the CMOS logic output; i.e. +5.0V and 0.5V (figure 6-14b). The high level corresponds to consecutive one's, whereas the low level corresponds to consecutive zero's. The decoder output is a stepwise triangular wave (figure 6-14c) at a fundamental frequency equal to that of the input. Figure 6-14c shows that, when the digital pattern is low, the stepwise triangular wave rises and vice versa. This because the decoder output is 180^o out of

phase with respect to its input. At slope overloading, an additional phase shift angle ϕ is introduced to the decoded wave (see figure 6-14). The amount of the angle ϕ depends upon the companding algorithm in the feedback. The total phase shift of the decoded wave under grossly slope overloading condition is then $\pi+\phi$. Figure 6-14 shows that the magnitude of ϕ is 108^{o}.

Figures 6-15, 6-16 and 6-17 corroborate the previous description of companding for the "step response" by showing that whenever the L(t) pattern changes its direction, companding starts with a larger step and then its magnitude decreases gradually at the successive sampling instants. Table 6-3 gives the step size Δ at each sampling period, the change between any two consecutive steps δ and the resulting amplitude of the decoded wave y(t) for three different ratios of $f_p/2f_s$. The table also shows that for a constant sampling rate f_p, the magnitude of the starting step is a function of the input signal frequency f_s.

This behaviour of the Harris device can be explained theoretically by examining its analogue equivalent circuit shown in figure 6-12. Assuming grossly slope overloading condition, figure 6-18 shows the expected waveforms at different points on the system. For the binary levels at the output of the encoder, the digital pattern L(t) (figure 6-18b) may be represented by:

$$L(t) = \begin{cases} V_H \text{ "1" state} & o \leq t \leq T_s/2 \\ V_L \text{ "0" state} & T_s/2 \leq t \leq T_s \end{cases} \qquad (6\text{-}2)$$



a) Sinusoidal analogue input.

b) Digital output.

c) Stepwise triangular decoded waveform.

Fig. 6-14 - Waveforms recorded by Harris CVSD modulation system under grossly slope overloading condition.

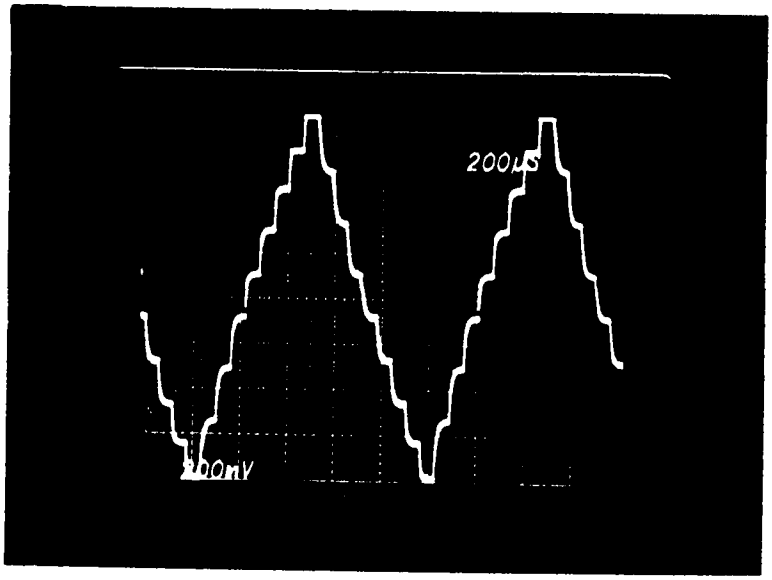


Fig. 6-15 - Stepwise triangular waveform at $f_p/f_s = 16$.

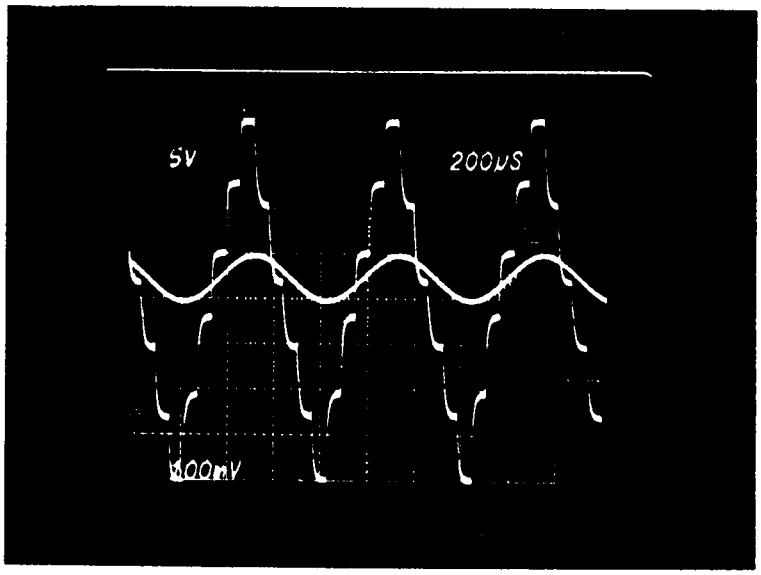


Fig. 6-16 - Stepwise triangular waveform at $f_p/f_s = 10$.

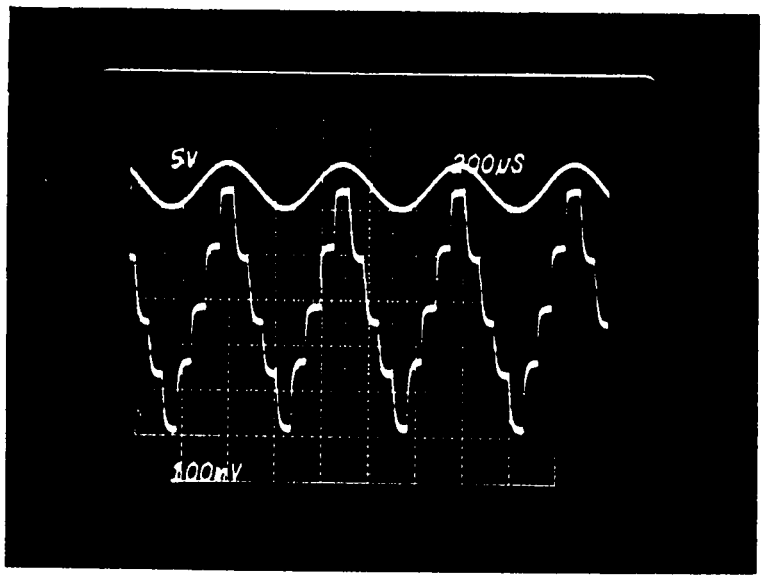
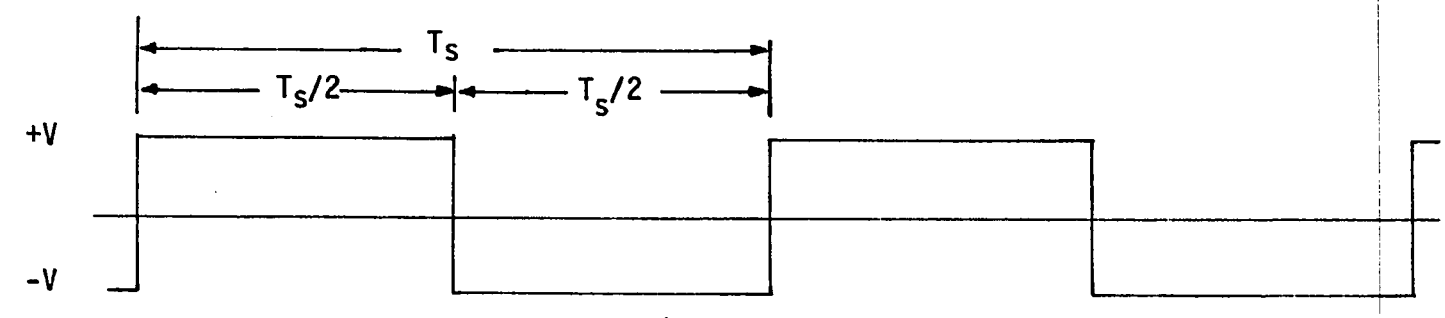


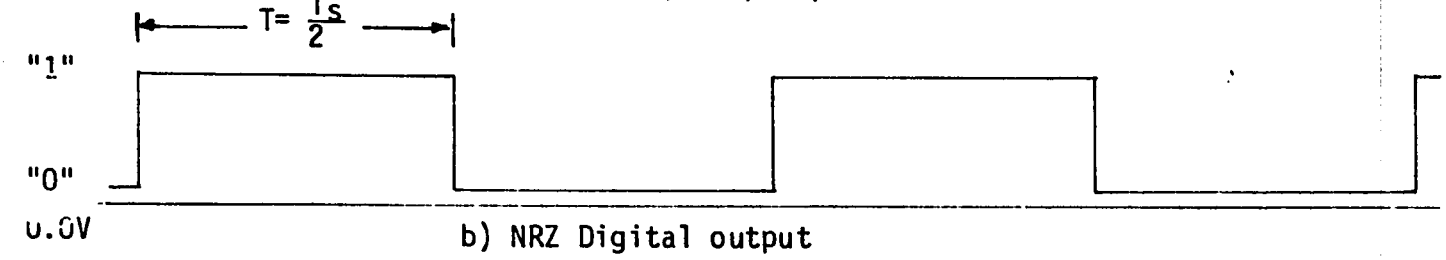
Fig. 6-17 - Stepwise triangular waveform at $f_p/f_s = 8$.

No. of step	f_p/f_s = 16.0			f_p/f_s = 10			f_p/f_s = 8.0		
	Step-size mv	Change in step-size mv	y(t) mv	Step-size mv	Change in step-size mv	y(t) mv	Step-size mv	Change in step-size mv	y(t) mv
1	260	-	260	190	-	190	160	-	160
2	240	20	500	175	15	365	145	15	305
3	220	20	720	160	15	525	130	15	435
4	200	20	920	145	15	670	115	15	550
5	190	10	1110	130	15	800			
6	180	10	1290						
7	170	10	1460						
8	140	30	1600						

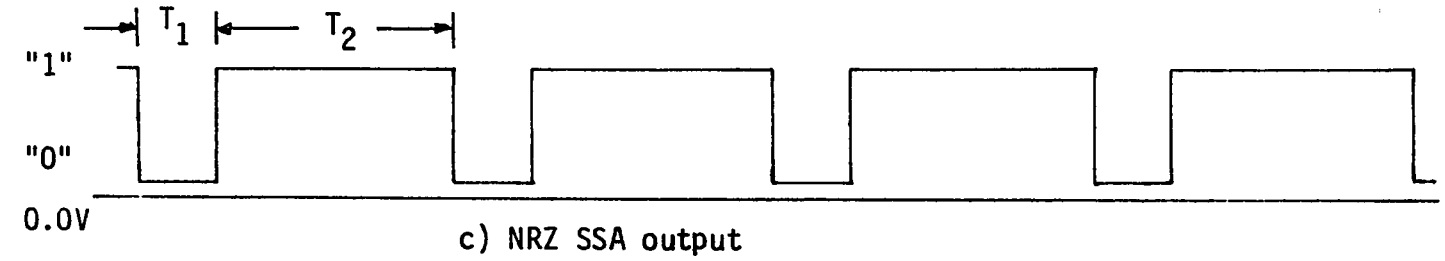
Table 6-3 - Magnitude of the feedback step-sizes at different ratios of f_p/f_s.



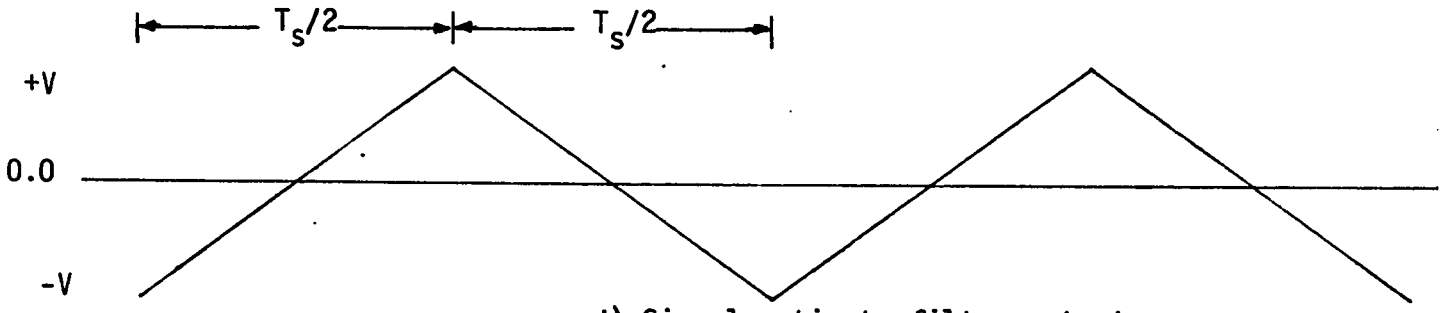
a) Step input



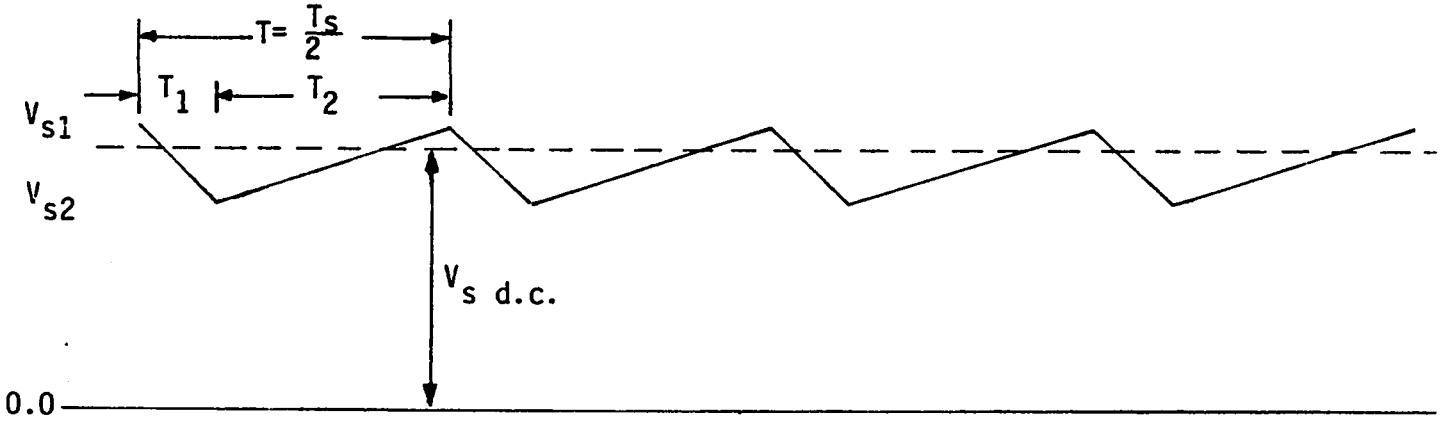
b) NRZ Digital output



c) NRZ SSA output



d) Signal estimate filter output



e) Syllabic filter output

Fig. 6-18 - Waveforms under grossly slope overloading condition at different points on the analogue equivalent of Harris device.

The signal slope analyzer output G(t) (figure 6-18c) activates when t is equal to or greater than $T_1 \geq nT_p$; i.e.:

$$G(t) = \begin{cases} V_L & \text{"0" state (inactive)} \quad 0 \leq t \leq T_1 \\ V_H & \text{"1" state (active)} \quad T_1 \leq t \leq T_2 \end{cases} \qquad (6\text{-}3)$$

Where: $T_1 = nT_p$ (n is the shift register length and T_p is the sampling period $1/f_p$).

$T_2 = T_s/2 - T_1$ (T_s is the period of the input signal; i.e. $1/f_s$)

The signal estimate filter output $V_E(t)$ (figure 6-18d) for such short time durations is nearly the integral of L(t). It rises when L(t) changes from "0" state to the "1" state and falls when the change is in the opposite direction. Actually the instantaneous behaviour of the rise or the fall is given by:

$$V_E(t) = V(1 - e^{-t/\tau_E}) + V_{E_o} e^{-t/\tau_E} \qquad (6\text{-}4)$$

Where: V_{E_o} is the voltage on capacitor C_E at t=0

$\tau_E = R_E C_E$ is the time constant of signal estimate filter and V is the total change (magnitude and polarity) of the encoder output.

If L(t) changes from "0" to "1" state, V is a positive quantity and $V_E(t)$ rises. For the opposite change of the L(t), V is a negative quantity and

$V_E(t)$ declines. At $t = \frac{T_s}{2}$, the total change in $V_E(t)$; i.e. the peak-to-peak amplitude of signal estimate filter output is:

$$V_E(T_s) = (V - V_{E_o}) (1 - e^{-\frac{T_s}{2\tau_E}}) \qquad (6\text{-}5)$$

For the grossly slope overloading condition, the peak-to-peak amplitude of $V_E(t)$ is inversely proportional to the frequency of the input signal f_s.

The output of the syllabic filter is a d.c. voltage. The syllabic capacitor charges after all shift register entries become "1" and discharges for a duration of nT_p, whenever L(t) changes its value (figure 6-18e). The effect of charging and discharging is to change the d.c. level at the syllabic filter output. During the discharging period, the instantaneous change in $V_s(t)$ is:

$$V_s(t) = V_{s1} e^{-t/\tau_s} \qquad (6\text{-}6)$$

Where: $\tau_s = R_s C_s$ is the time constant of the syllabic filter and V_{s1} is the voltage on C_s at t=0. If the input signal is constant in amplitude and frequency, $V_s(t)$ is periodic and:

$$V_s(T_1) \backsimeq V_{s2} = V_{s1} e^{-T_1/\tau_s} \qquad (6\text{-}7)$$

During the charging period the instantaneous behavior of $V_s(t)$ is:

$$V_s(t) = V_s(1 - e^{-t/\tau_s}) + V_{s_2} e^{-t/\tau_s} \qquad (6\text{-}8)$$

Where: V_s is the input at the syllabic filter input (high level of SSA output).

For a charging period of T_2:

$$V_s(T_2) = V_s(1 - e^{-T_2/\tau_s}) + V_{s2}\, e^{-T_2/\tau_s} \simeq V_{s1}$$

Because τ_s is very large (4m sec for the Harris) device, $V_{s1} \simeq V_{s2}$. That is it is nearly a d.c. value depending on the values of T_1 and T_2. Furthermore $T_1+T_2=T_s/2$, which implies $V_s(DC)$ depends on $T_s=(1/f_s)$. It is through this that $B(f_s)$ is determined. The relationships will be derived later.

The feedback signal was expressed previously as:

$$V_f(t) = [A + B(f_s)]\ V_E(t) \qquad (6\text{-}9)$$

Then substituting for $V_E(t)$ from 6-4:

$$V_f(t) = [A + B(f_s)]\ [V(1 - e^{-t/\tau_E}) + V_{E_o}\, e^{-t/\tau_E}] \qquad (6\text{-}10)$$

For a certain input frequency, f_s satisfying grossly slope overloading, the peak-to-peak amplitude of $V_f(t)$ is:

$$V_f(T_s) = [A + B(f_s)]\ [(V - V_{E_o})(1 - e^{-T_s/2\tau_E})] \qquad (6\text{-}11)$$

At grossly slope overloading $T_s = \frac{f_p}{f_s} T_p$, then

$$V_f(T_s) = V_{E_p}[A + B(f_s)]\ (1 - e^{-\frac{f_p T_p}{2 f_s \tau_E}}) \qquad (6\text{-}12)$$

Where $V_{E_p} = (V - V_{E_o})$

Differentiating 6-12 with respect to T_p, results in the step size variation with consecutive sampling periods; i.e.:

$$\frac{dV_f(T_s)}{dT_p} = V_{E_p}[A + B(f_s)]\ e^{-\frac{NT_p}{\tau_E}} \qquad (6\text{-}13)$$

Where: $N = \frac{f_p}{2f_s}$, which determines number of consecutive "1's"or consecutive "0's" in L(t) pattern under slope overloading condition.

Equation 6-13 indicates that step size per sampling period decays exponentially. It has the greatest magnitude for the starting step and the following steps decrease gradually. The amount of decrement; i.e. the difference between any two consecutive steps is exponential. As an approximation, if the series form of an exponential is used; i.e. |18|:

$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + \ldots.$$

Then:

$$e^{-\frac{N}{\tau_E} T_p} = 1 - \frac{N}{\tau_E} T_p + \frac{(NT_p)^2}{2!\tau_E^2} - \frac{(NT_p)^3}{3!\tau_E^3} + \ldots.. \qquad (6\text{-}14)$$

Where $N = 0, 1, 2, 3, \ldots\ (\frac{f_p}{2f_s} - 1)$

If $T_p << \tau_E$, then the third and higher terms can be ignored and equation 6-14 yields:

$$\frac{dV_f(T_s)}{dT_p} \simeq V_{E_p}[A + B(f_s)] \left(1 - \frac{N}{\tau_E} T_p\right) \qquad (6\text{-}15)$$

Observe that step size decreases with N. Table 6-4 gives step sizes at consecutive sampling periods, using equation 6-13 and 6-15 and assuming $f_p/2f_s = 8$ and $\tau_E = 1.0$m sec. The percentage error in the step size, due to the approximation, is also given in this table. The error is greater for larger N. This is because the neglected terms in equation 6-14 (especially the third term) become comparable with the second term. However, the approximation is quite good for low ratios of $f_p/2f_s$.

From equation (6-13) the magnitude of the starting step Δ_o is given by:

$$\Delta_o = V_{E_p}[A + B(f_s)] \qquad (6\text{-}16)$$

Equation 6-16 indicates that the magnitude of the starting step under grossly slope overloading condition is a function of $B(f_s)$. Experimental data has shown that when the system is just completely slope overloaded, $B(f_s)$ has its maximum value. As f_s increases, $B(f_s)$ and Δ_o decrease accordingly. The rate at which the starting step Δ_o changes with frequency will now be theoretically determined.

Step No.	Actual step size		Approximate step size		% difference between Δ and Δ' w.r.t. Δ
	Δ	δ	Δ'	δ'	
Δ_0	$V[A+B(f_s)]$		$V[A+B(f_s)]$		0.0
Δ_1	$0.939\ \Delta_0$	0.0605	$0.9375\ \Delta_0$	0.0625	0.2
Δ_2	$0.8825\ \Delta_0$	0.0569	$0.875\ \Delta_0$	0.0625	0.85
Δ_3	$0.829\ \Delta_0$	0.05347	$0.8125\ \Delta_0$	0.0625	1.99
Δ_4	$0.779\ \Delta_0$	0.0502	$0.7500\ \Delta_0$	0.0625	3.72
Δ_5	$0.732\ \Delta_0$	0.0472	$0.6875\ \Delta_0$	0.0625	6.08
Δ_6	$0.687\ \Delta_0$	0.0443	$0.625\ \Delta_0$	0.0625	9.025
Δ_7	$0.7456\ \Delta_0$	0.0416	$0.5625\ \Delta_0$	0.0625	12.9

Table 6-4 - Real and approximate step size variation with consecutive sampling period at slope overloading condition.

Figure 6-19 shows the signal slope analyzer output and the variation of the d.c. level due to the charging and discharging of the capacitor C_s. The syllabic voltage $V_s(t)$ at the end of the discharging period T_1 was given by equation 6-7; i.e.:

$$V_s(T_1) \simeq V_{s2} = V_{s1}\, e^{-T_1/\tau_s} \simeq V_{s1}\,(1 - \frac{T_1}{\tau_s}) \qquad (6\text{-}17)$$

During the charging period T_2:

$$V_s(T_2) = V_s(1 - e^{-T_2/\tau_s}) + V_{s2}\, e^{-T_2/\tau_s}$$

$$= V_{s1} \simeq V_s \frac{T_2}{\tau_s} + V_{s2}\,(1 - \frac{T_2}{\tau_s}) \qquad (6\text{-}18)$$

The effect of charging and discharging is to produce a new d.c. level; i.e.:

$$V_{sDC} = V_{s2} + \frac{(T_1+T_2)\,(V_{s1}-V_{s2})}{2(T_1+T_2)}$$

But for the triangular variation:

$$V_{sDC} = \frac{V_{s1} + V_{s2}}{2} \qquad (6\text{-}19)$$

Substituting 6-17 in 6-18, V_{s1} in term of V_s yields:

$$V_{s1} = V_s \tau_s \frac{T-T_1}{T\tau_s - T_1(T-T_1)} \qquad (6\text{-}20)$$

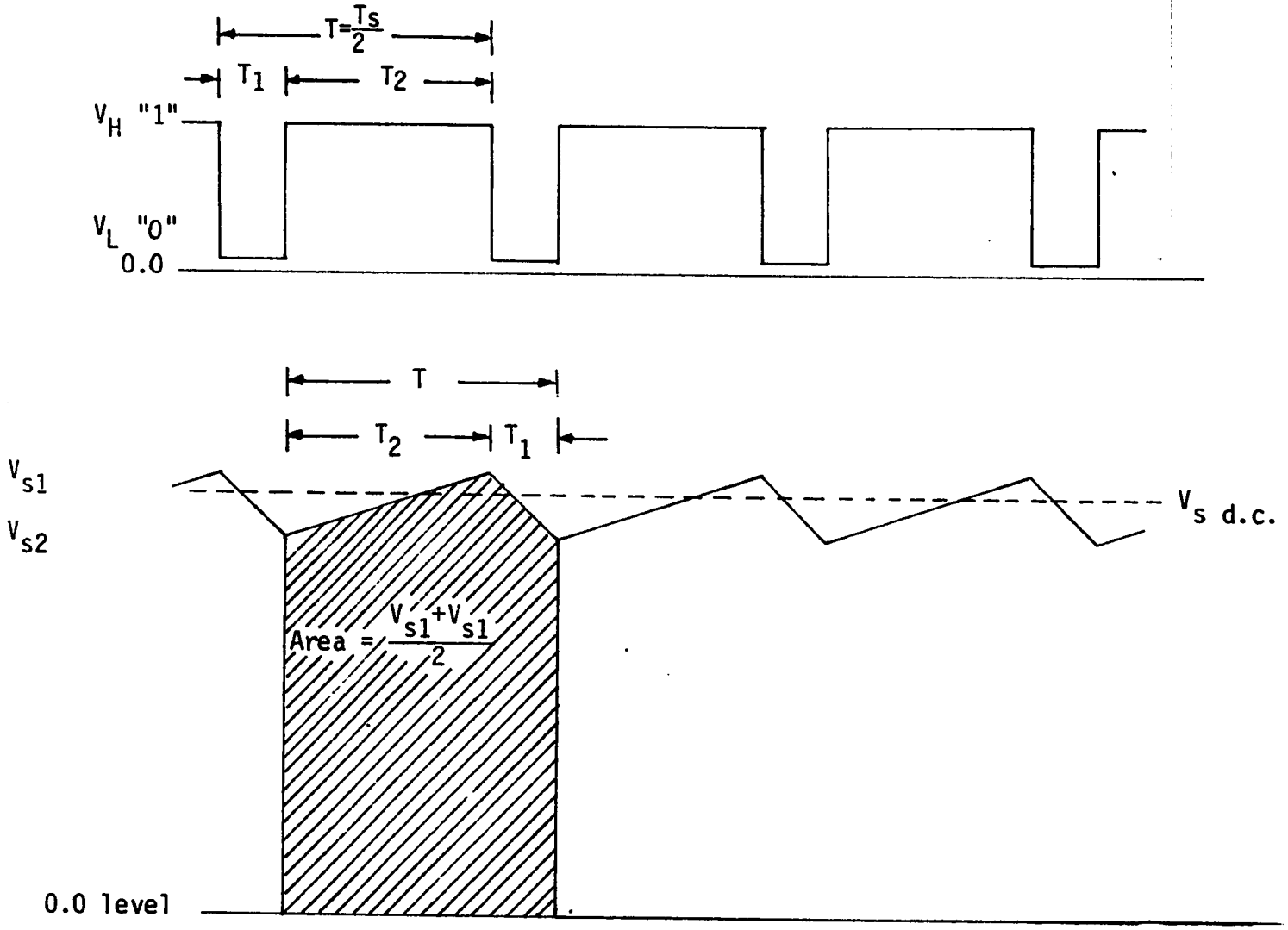


Fig. 6-19 - Variation of the DC with input frequency f_s at the syllabic filter output.

Now V_{s2} in term of V_s is:

$$V_{s2} = V_s\tau_s \frac{T-T_1}{T\tau_s-T_1(T-T_1)} \cdot (1 - \frac{T_1}{\tau_s}) \qquad (6\text{-}21)$$

Then V_{sDC} in term of V_s is:

$$V_{sDC} = V_s\tau_s \frac{T-T_1}{T\tau_s-T_1(T-T_1)} (2 - \frac{T_1}{\tau_s})$$

$$= V_s(2\tau_s-T_1) \frac{T-T_1}{T\tau_s-T_1(T-T_1)}$$

Or:

$$V_{sDC} = \frac{K}{\tau_s \frac{T}{T-T_1} - T_1} \qquad (6\text{-}22)$$

Where: $K = V_s(2\tau_s - T_1)$

Expressing 6-22 in frequency f_s, since $T = \frac{1}{2f_s}$, then:

$$V_{sDC} = \frac{K}{\frac{\tau_s}{1-2T_1f_s} - T_1} \qquad (6\text{-}23)$$

Equation 6-23 indicates that V_{sDC} approaches zero when as the value of the denominator grows larger. The limit is achieved when the term $(1-2T_1f_s)$ is zero; i.e. when

$$f_s = \frac{1}{2T_1} = \frac{1}{2nT_p} = \frac{f_p}{2n} \qquad (6\text{-}24)$$

Since n=2 in Harris device, then, V_{sDC}; i.e. $B(f_s)=0$ at $f_s=4.0$ KHZ for a sampling rate of 16.0 KHZ. The rate at which the starting step Δ_o changes with signal frequency under slope overloading condition is shown in figure 6-20. The experimental rate was obtained by measuring the starting step at different input frequencies (Table 6-5). The system was overloaded with a 5.0V peak-to-peak sinusoidal signal (the maximum allowable input amplitude). The frequency required to just slope overload the system with above input condition was found to be 550 HZ. Below this frequency the analysis of the starting step is therefore not applicable. The computed points on figure 6-20 were obtained according to the following concepts:

The magnitude of starting step Δ_o was given by:

$$\Delta_o = V_{EP}\,[A + B(f_s)]$$

Also, it was shown that $B(f_s)=0$ at $f_s=4.0$ KHZ, and therefore beyond 4.0 KHZ the peak-to-peak amplitude of the decoded will be as its idling condition; i.e.

$$V_f(t) = AV_{Ep}(1 - e^{-t/\tau_E}) \qquad (6\text{-}25)$$

Since at idling the frequency of L(t) is $\frac{f_p}{2}$; i.e. $t=2T_p$, then:

$$V_f(2T_p) = AV_{Ep}\,(1 - e^{-\frac{2T_p}{\tau_E}})$$

$$\frac{dV_f(2T_p)}{dT_p} = AV_{Ep}\; e^{-\frac{2T_p}{\tau_E}} \qquad (6\text{-}26)$$

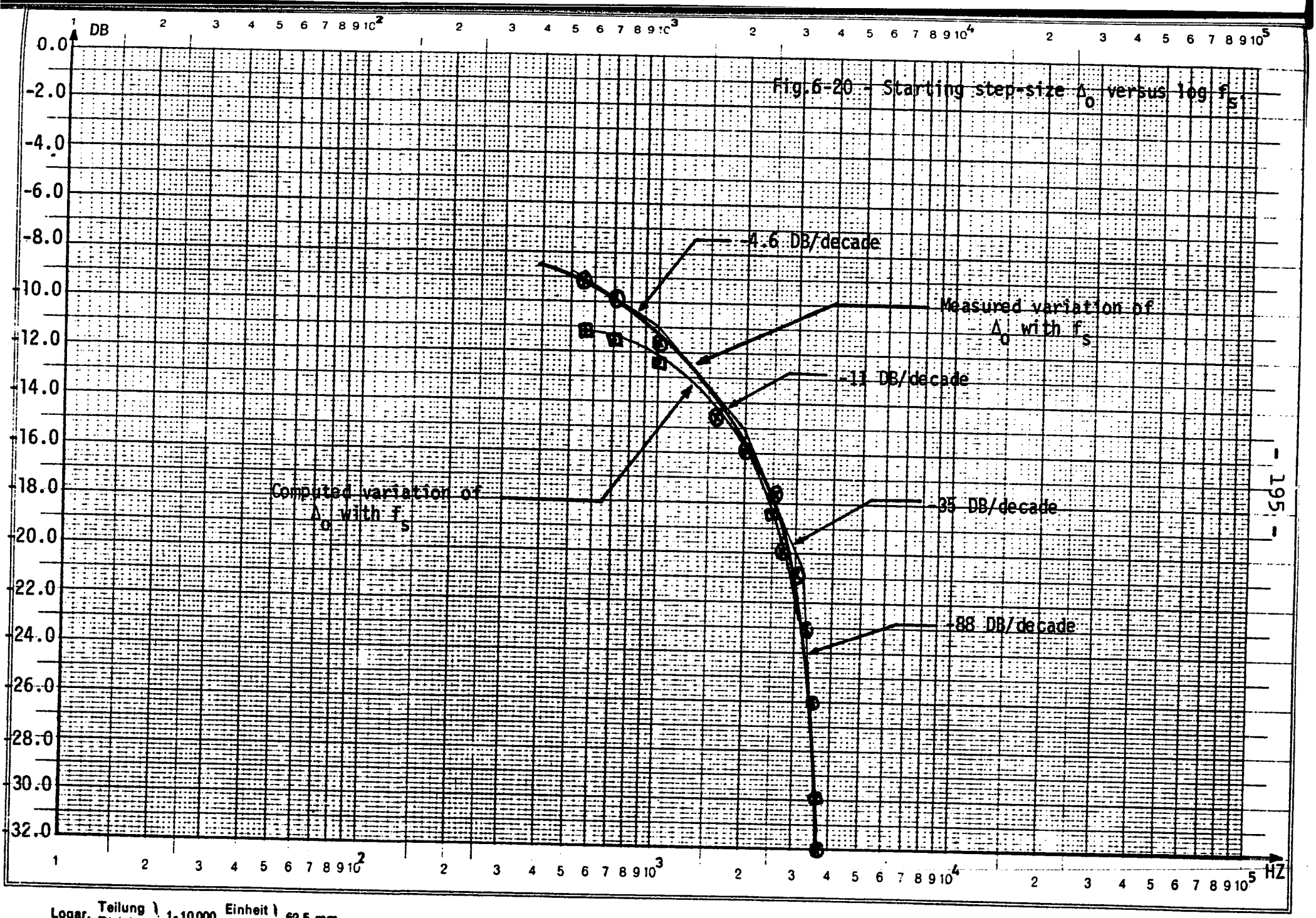


Fig.6-20 - Starting step-size Δ_o versus log f_s

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Ed. Aerni-Leuch, Bern Nr. 526

Frequency HZ	Starting step magnitude Δ_o	
	mv	20 log Δ_o DB
550	350	-9.1
700	320	-9.9
1000	260	-11.7
1600	190	-14.4
2000	160	-15.9
2500	130	-17.7
2700	100	-20.0
3000	90	-20.9
3250	70	-23.1
3500	50	-26.0
3700	25	-32.0
4000	14	-37.0

Table 6-5 - Measured starting step-size at different input frequencies.

At idling, the decoded signal changes by one step whenever L(t) changes its state. Therefore the starting step at idling is equal to the peak-to-peak amplitude of the idling pattern; i.e:

$$\Delta_{idle} = AV_{Ep} = 14 \text{ mv} \tag{6-27}$$

Now the magnitude of starting step at any frequency below 4.0 KHZ can be written as:

$$\Delta_o = \Delta_{idle} + V_{Ep}B(f_s)$$

Or:

$$\Delta_o - \Delta_{idle} = V_{Ep}B(f_s) = \frac{\frac{V_{EP}K}{\tau_s}}{1 - \frac{1}{2T_1 f_s} - T_1} \tag{6-28}$$

Because of unknown constants, this is still inadequate information to compute the points through which a curve for equation (6-28) will pass. However, a comparison of curvature is possible. This can be accomplished by further assuming that the computed curve will pass through a point of the measured data. This has been done for f_s = 2.0 KHZ. Using τ_s = 4m sec and $T_1 = nT_p = \frac{2}{f_p}$ = 0.125m sec in equation 6-28, the value of the constant $V_{EP}K$ yields 1.1498×10^{-3}. It is now possible to employ equation 6-28 for computing the magnitude of the starting step at different input frequencies (table 6-6). The

f_s HZ	$\frac{\tau_s}{1-2T_1 f_s}$	$\frac{\tau_s}{1-2T_1 f_s} - T_1$	$VB(f_s) = \frac{VK}{\frac{\tau_s}{1-2T_1 f_s} - T_1}$	$\Delta_o = AV + VB(f_s)$	
				mv	20 log Δ_o DB
550	4.6377×10^{-3}	4.5127×10^{-3}	255 mv	269	-11.4
700	4.8484×10^{-3}	4.7234×10^{-3}	243 mv	257	-11.8
1.0K	5.333×10^{-3}	5.2083×10^{-3}	221 mv	235	-12.6
1.6K	6.6667×10^{-3}	6.5417×10^{-3}	176 mv	190	-14.4
2.0K	8.0×10^{-3}	7.875×10^{-3}	146 mv	160	-15.9
2.5K	10.667×10^{-3}	10.542×10^{-3}	109 mv	123	-18.2
2.7K	13.0×10^{-3}	12.875×10^{-3}	89 mv	103	-19.7
3.0K	16.0×10^{-3}	15.875×10^{-3}	72 mv	86	-21.3
3.25K	21.333×10^{-3}	21.2083×10^{-3}	54 mv	68	-23.3
3.5K	32.0×10^{-3}	31.875×10^{-3}	36 mv	50	-26.0
3.7K	53.333×10^{-3}	53.208×10^{-3}	22 mv	36	-29.0
4.0K	∞	∞	0.0 mv	14	-37.0

$T_1 = nTP = \frac{2}{f_p} = 0.125$m sec at f_p=16.0 KHZ

τ_s = 4.0m sec. AV = 14 mv

$V_K = 1.1498 \times 10^{-3}$

Table 6-6 - Computation of starting step at different input frequencies f_s.

deviation between the measured and the computed values of Δ_o in figure 6-20 is more significant for frequencies below 2.0 KHZ than those above 2.0 KHZ. This deviation could be due to the assumptions of a constant d.c. value and linearization of the exponential equation. One expects that the error in these assumptions will become greater for lower f_s. Better results could be achieved by using an instantaneous value of $V_s(t)$ and assuming exponential variations.

Both curves (measured and computed) show that the variation of the starting step with frequency in log scale is highly nonlinear over the entire slope overloading region from 550 to 4000 HZ. The assymptotic approximation of the experimental curve shows that magnitude of Δ_o changes at a rate of:

- 4.6 dB/decade from 550 to 1000 HZ
-11.0 dB/decade from 1000 to 2000 HZ
-35.0 dB/decade from 2000 to 3250 HZ
-88.0 dB/decade from 3250 to 4000 HZ

The fast drop above 2.0 KHZ is due to the property of the shift register algorithm in the SSA network; i.e. above 2 KHZ the charging period of C_s becomes smaller than of the discharging period and consequently $B(f_s)$ falls very rapidly. This was explained in chapter-5 for the Motorola device.

The frequency spectrum of the stepwise triangular waveform (figure 6-21 and 6-22) shows the fundamental and its odd harmonics according to the Fourier series expansion of a triangular wave. Theoretically expected amplitudes and the measured ones are tabulated in table 6-7. The larger errors for the higher harmonics (7th to 13th) is due to the superimposing effect of the lower side-band harmonics of the first overtone component (figure 6-23) which occurs at a nearby frequency. Figure 6-24 shows the overtone components together with their both upper and lower side bands harmonics translated by the sampling rate and its multiples. Table 6-8 compares these overtone peaks with the measured fundamental peak.

Because of low frequency distortion at slope overloading, the output of the low-pass filter will not adequately attenuate the noise. This noise is greater than the noise in the normal operating condition and is referred to as "slope overloading noise".

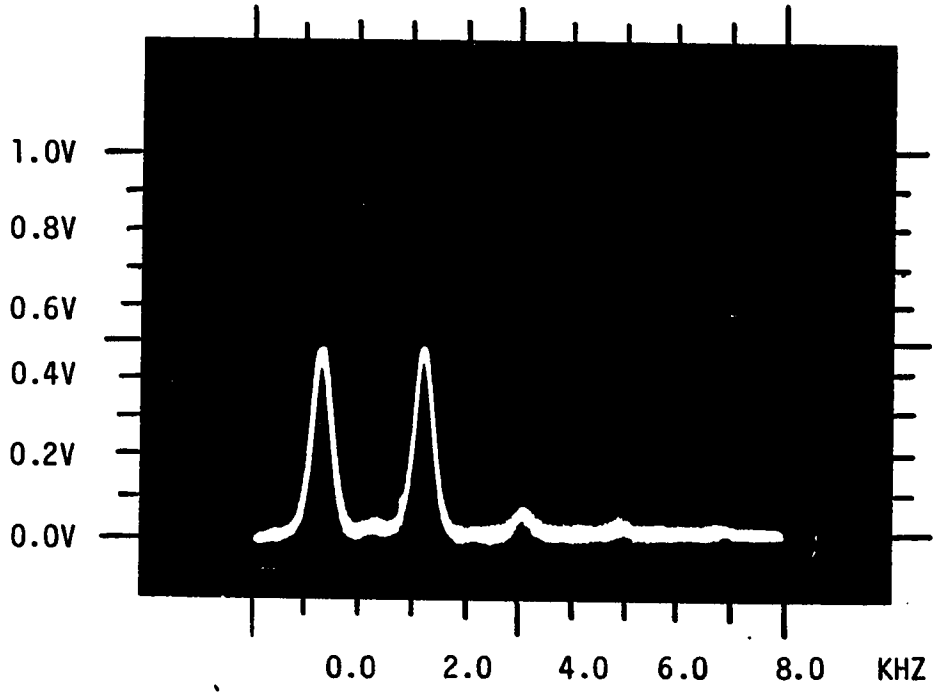

Fig. 6-21 - Frequency spectrum of the decoded wave (stepwise triangular) under grossly slope overloading condition.

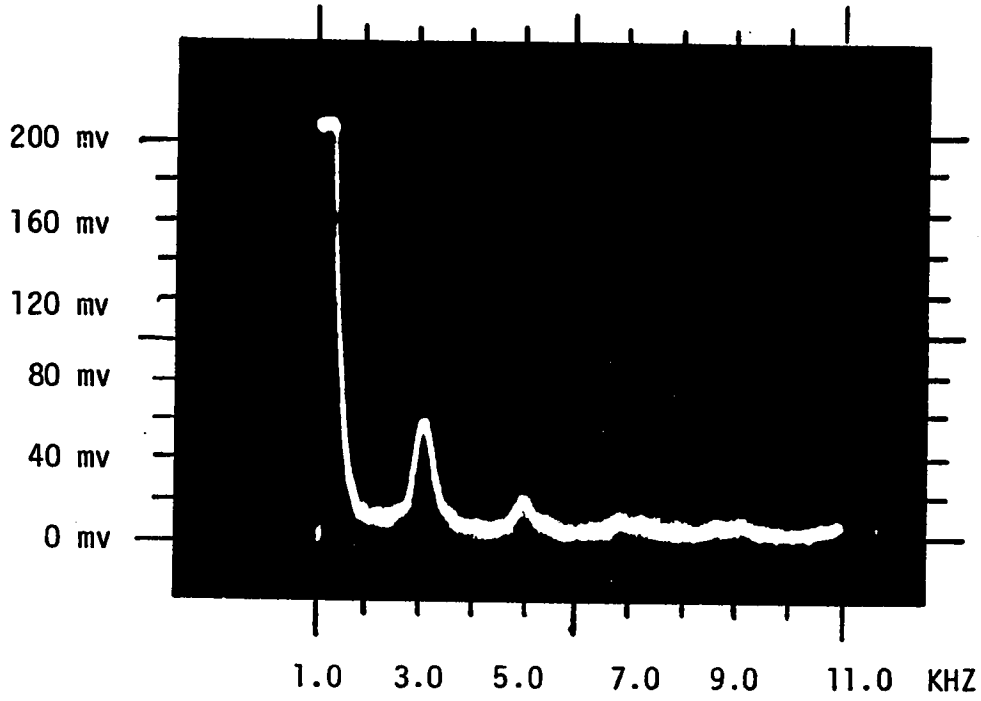

Fig. 6-22 - Frequency spectrum of the stepwise triangular wave showing several odd harmonics.

n	Computed peaks $\frac{8A}{\pi^2 n^2}$ mv	Frequency KHZ	Measured peaks mv	% difference w.r.t. the computed peak
1	689.0	1.0	665.0	-3.5
3	77.0	3.0	82.0	6.5
5	28.0	5.0	28.3	1.0
7	14.0	7.0	17.0	21.4
9	8.5	9.0	14.0	64.7
11	5.7	11.0	17.0	198.0
13	4.0	13.0	19.8	395.0

Measured value of A = 0.85V (peak) from figure 6-14c.

Table 6-7 - Computed and measured amplitudes of the harmonics of the triangular decoded waveform.

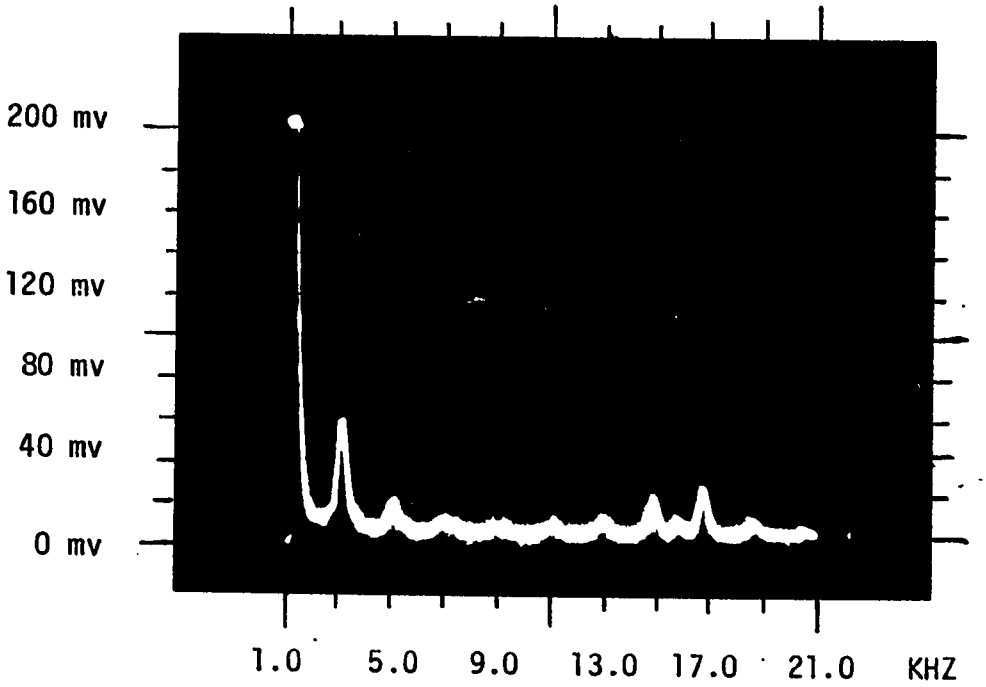

Fig. 6-23 - Frequency spectrum of the stepwise decoded wave over a wider frequency range. First overtone component at 16 $\pm$ 1.0 KHZ also appears in this figure.

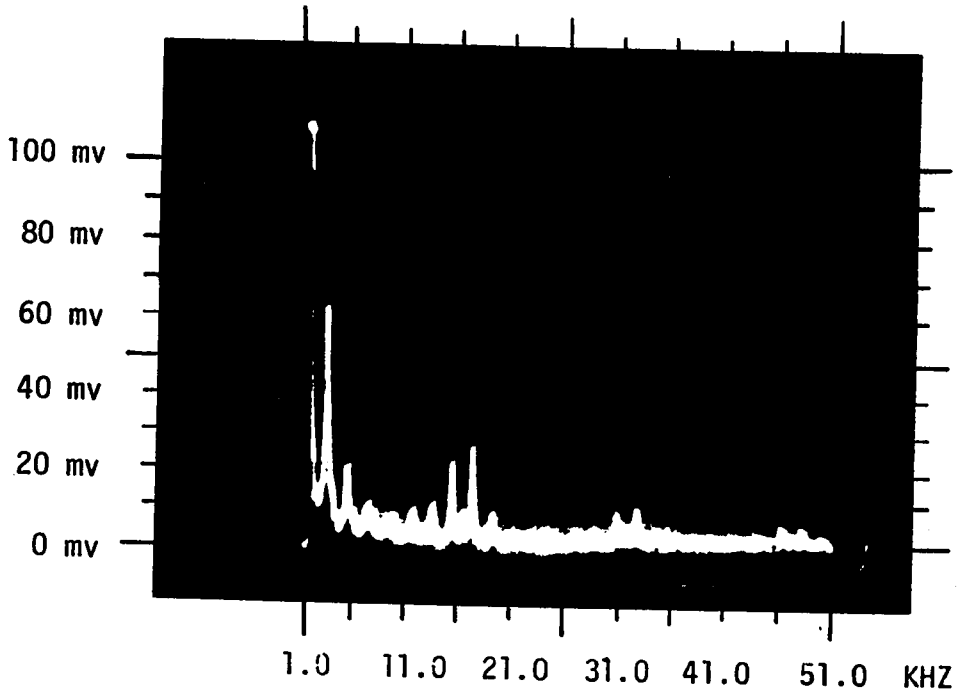

Fig. 6-24 - Overtone components at the consecutive multiples of sampling rate f_p and their accompanied side bands harmonics.

Overtone peak No.	Frequency KHZ	Amplitude mv	% amplitude w.r.t. the fundamental
1st	16.0 ± 1.0	28.3	4.25
2nd	32.0 ± 1.0	12.7	1.90
3rd	48.0 ± 1.0	7.0	1.06

Fundamental peak = 665 mv at 1.0 KHZ.

Table 6-8 - Overtone components peaks and their percentage amplitudes w.r.t. the fundamentals.

6-6 - Frequency response

Theoretical prediction of the transfer function characteristic is possible through analysis of the concluded algorithm, which determines the starting step at slope overload from f_s (figure 6-20). Also it was shown on table 6-4, that the change between any two consecutive step sizes is nearly a fixed value defined by δ. Assuming a permanent slope overloading condition, at each input frequency f_s, the corresponding value of the starting step (Δ_0) is obtained from figure 6-20. The successive values of the steps are obtained by by subtracting a fixed amount (δ) from the preceding step-size such that:

$$\Delta_1 = \Delta_0 - \delta$$

$$\Delta_2 = \Delta_1 - \delta = \Delta_0 - 2\delta$$

$$\Delta_3 = \Delta_2 - \delta = \Delta_0 - 3\delta$$

$$\Delta_r = \Delta_{r-1} - \delta = \Delta_0 - r\delta \qquad (6\text{-}29)$$

Where: $r = 1,2,\ldots N-1$ and $N = f_p/2f_s$ (Assuming a symmetrical encoder, the number of one's is equal to the number of zero's at the output of the encoder.)

The peak-to-peak amplitude of the stepwise decoded wave is therefore simply the summation of these step sizes; i.e.:

$$y(t)_{p-p} = \sum_{r=0}^{N-1} \Delta_r \qquad (6\text{-}30)$$

The algorithm described above was used to predict the transfer function characteristics of the HC55516 device. Assuming that δ = 14 mv; i.e. the minimum value of the step size produced at the output of the decoder at idling condition. The fundamental of the Fourier series expansion of the triangular wave was considered as the pure decoded signal at the output of the decoder. Table 6-9 gives the required data to obtain such characteristics. The theoretically predicted characteristic (figure 6-25) gives asymptotic results and has a slope of -13DB/octave. The cut-off frequencies are obtained by the projection of the -3DB level of an assumed input signal with the predicted asymptotic beyond the -3DB frequency.

f_s HZ	$f_p/2f_s$	$y(t)_{p-p}$ * V	Fundamental p-p output $= 8/\pi^2\ y(t)$	
			V	DB **
400	20	4.78	3.87	-0.29
500	16	4.0	3.24	-1.82
800	10	2.39	1.94	-6.3
1000	8	1.77	1.43	-8.91
1600	5	0.88	0.71	-15.0
2000	4	0.58	0.47	-18.6

* The detail of y(t) is given in table 6-10.

** Relative to 4.0V p-p as 0.0 DB

Table 6-9 - Theoretically computed data for the amplitude response of HC-55516 device.

No. of step r	Step-size Δ at consecutive sampling instants r for different ratios $f_p/2f_s$ = N					
	20	16	10	8	5	4
0	372	355	302	270	204	166
1	358	341	288	256	190	152
2	344	327	274	242	176	138
3	330	313	260	228	162	124
4	316	299	246	214	148	
5	302	285	232	200		
6	288	271	218	186		
7	274	257	204	172		
8	260	243	190			
9	246	229	176			
10	232	215				
11	218	201				
12	204	187				
13	190	173				
14	176	159				
15	162	145				
16	148					
17	134					
18	120					
19	106					
$y(t)_{p-p} \sum_{r=0}^{N-1} \Delta_r$	4.78V	4.0V	2.39V	1.768V	880 mv	580 mv

Table 6-10 - Theoretically expected peak-to-peak amplitude of the stepwise triangular waveform at different ratios $f_p/2f_s$.

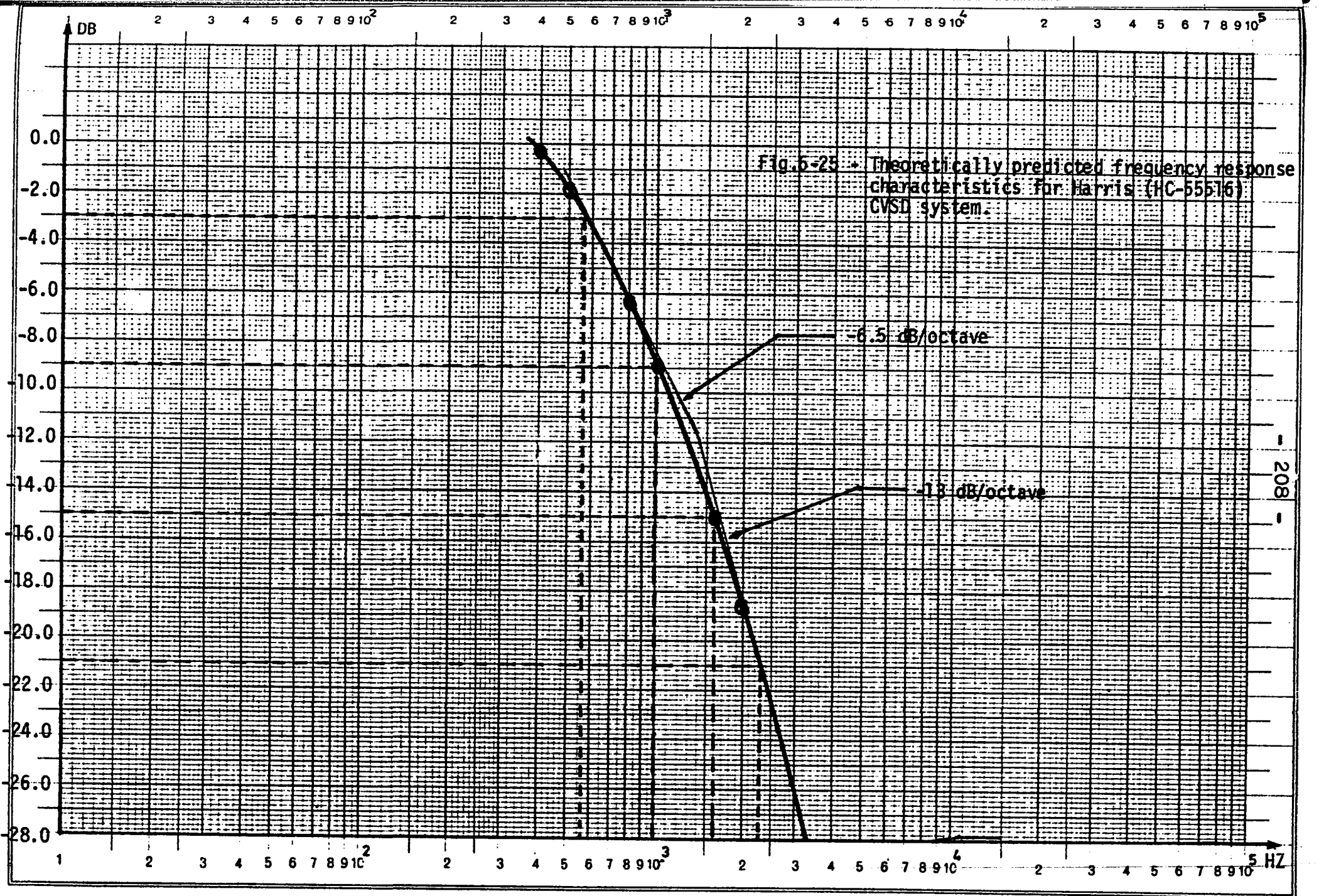

Fig.6-25 : Theoretically predicted frequency response characteristics for Harris (HC-55516) CVSD system.

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The experimentally obtained transfer function characteristic of the HC-55516 (CVSD) modulation system is shown in figure 6-26. The required data for this figure were obtained by reading the fundamental peak from the frequency spectrum display of the stepwise decoded waveform (table 6-11). Within the tracking region, the pure decoded signal is slightly lower than the input due to the smoothing process performed by the spectrum analyzer. At slope overloading, the fundamental of the Fourier series expansion of the stepwise triangular wave was considered as the pure decoded signal. The rate at which the output changes with the input frequency f_s is approximately-13DB/octave (-43DB/decade). Comparing the cut-off frequencies obtained from the transfer function characteristic published by the manufacturer (figure 6-27) |26| with those obtained theoretically and experimentally (table 6-12) shows that the resulting values are very close to each other. The experimentally evaluated cut-off frequencies differ by a maximum of 7.7 percent with those published by the manufactuere and by a maximum of 9.8 percent with those obtained experimentally. This small variation in the cut-off frequencies hardly supports the validity of the approach used in determining the transfer function characteristic.

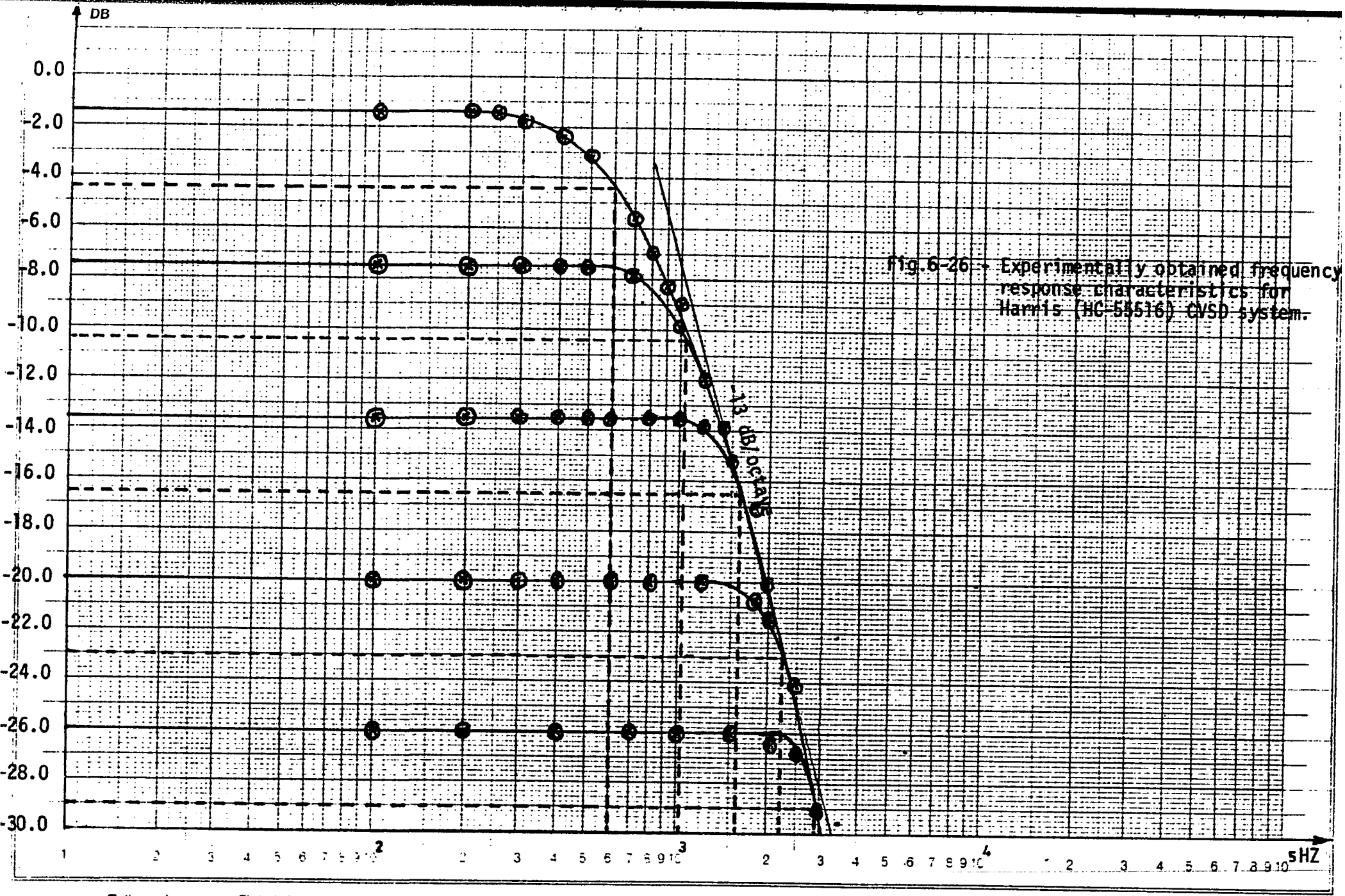

Fig.6-26 - Experimentally obtained frequency response characteristics for Harris (HC-55516) CVSD system.

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Input frequency f_s HZ	4.0 p-p input 0.0 dB		2.0v p-p input -6.0 dB		1.0v p-p input -12.0 dB		0.5v p-p input -18.0 dB		0.25v input -24.0 dB	
	Peak output		Peak output		Peak output		Peak output		Peak output	
	volt	dB	volt	dB	volt	dB	volt	dB	volt	dB
100	1.70	-1.4	0.85	-7.5	0.42	-13.5	0.2	-20.1	0.1	-26.1
200	1.70	-1.4	0.85	-7.5	0.42	-13.5	0.2	-20.1	0.1	-26.1
250	1.70	-1.4	0.85	-7.5	0.42	-13.5	0.2	-20.1	0.1	-26.1
300	1.6	-1.8	0.85	-7.5	0.42	-13.5	0.2	-20.1	0.1	-26.1
400	1.5	-2.3	0.85	-7.5	0.42	-13.5	0.2	-20.1	0.1	-26.1
500	1.4	-3.2	0.85	-7.5	0.42	-13.5	0.2	-20.1	0.1	-26.1
700	1.1	-5.5	0.82	-7.7	0.42	-13.5	0.2	-20.1	0.1	-26.1
800	0.9	-7.0	0.82	-7.7	0.42	-13.5	0.2	-20.1	0.1	-26.1
900	0.8	-8.2	0.76	-8.4	0.42	-13.5	0.2	-20.1	0.1	-26.1
1000	0.71	-9.0	0.68	-9.9	0.42	-13.5	0.2	-20.1	0.1	-26.1
1200	0.51	-11.9	0.51	-11.9	0.41	-13.8	0.2	-20.1	0.1	-26.1
1400	0.41	-13.8	0.41	-13.8	0.37	-14.7	0.18	-20.7	0.1	-26.1
1500	0.35	-15.1	0.35	-15.1	0.35	-15.1	0.18	-20.7	0.1	-26.1
1800	0.28	-17.0	0.28	-17.0	0.28	-17.0	0.18	-20.7	0.1	-26.1
2000	0.23	-19.0	0.23	-19.0	0.23	-19.0	0.17	-20.7	0.09	-27.7
2200	0.17	-21.4	0.17	-21.4	0.17	-21.4	0.17	-21.4	0.08	-28.2
2500	0.13	-24.0	0.13	-24.0	0.13	-24.0	0.13	-24.0	0.071	-29.0
3000	0.071	-29.0	0.071	-29.0	0.071	-29.0	0.071	-29.0	0.064	-29.9
3500	0.028	-37.0	0.028	-37.0	0.028	-37.0	0.028	-37.0	0.028	-37.0

Table 6-11 - Measured frequency response data.

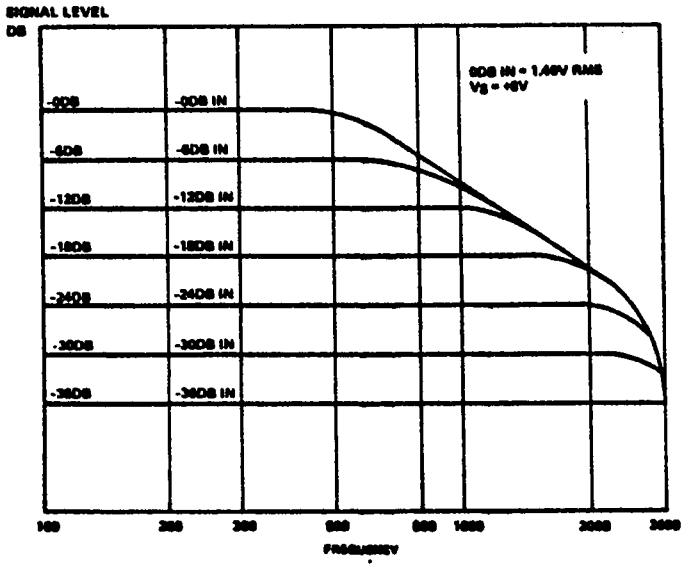

Fig. 6-27 - Published frequency response characteristic for Harris (HC-55516) CVSD system.

Input level DB	Cut-off frequencies			% difference	
	Theoretically HZ	Experimentally HZ	Published HZ	Experimental w.r.t. Theoretical	Experimental w.r.t. Published
0.0	665	600	650	-9.8	-7.7
-6.0	1000	1050	1000	5.0	5.0
-12.0	1600	1600	1650	0.0	-3.0
-18.0	2270	2200	2100	3.1	4.8

Table 6-12 - Theoretical, experimental and published cut-off frequencies.

CHAPTER - 7
CONCLUSIONS AND FUTURE WORK

7-1 Conclusions

By comparing the test results of the three tested systems (linear and CVSD modulation systems,using Motorola and Harris devices), the following conclusions are made:

1- The performance of the LDM system is a function of its feedback loop gain (step-size) and the sampling rate f_p. The maximum amplitude of the analogue input signal E_{sm} (dynamic range) and its bandwidth characteristic can be controlled by changing either the step-size (Δ), the sampling rate (f_p), or both. The dynamic range and the bandwidth are directly proportional to the variation of the step-size and the sampling rate (see equation 1-8).

2- A similar conclusion is also applicable for the CVSD system; i.e. the performance of the system is a function of loop gain and sampling rate. But since, the loop gain of the syllabically companded system is a variable quantity and is inversely proportional to the syllabic filter time constant. This leads to a conclusion that the performance of the CVSD system will be degraded as the syllabic filter time constant is made larger.

3- The transfer function characteristic of a CVSD system is also affected by the shift register length (n) used

in the SSA algorithm. The total bandwidth of the system becomes narrower as the size of the shift register increases.

4- Companded systems provide much wider dynamic range and bandwidth than an LDM system. This was corroborated by comparing the transfer function characteristic of the LDM system with the characteristics of CVSD systems, using the Harris and the Motorola devices. Table 7-1 indicates that, with respect to the LDM system, an improvement in the bandwidth from 9.0% to 130% was gained by the Harris device. Motorola devices provide much larger bandwidths. Again with respect to the LDM system, an improvement from 57% to 996% and from 23% to 765% was obtained using the MC-3417 and the MC-3418 devices, respectively. The improvement of course is a consequence of the companding process. The percentage of improvement is less as the amplitude of the input signal decreases. This arises from the difference in the "roll-offs" of the transfer function characteristics of each system. Figure 7-1 illustrates this property graphically for the LDM and the Harris CVSD system.

5- The noise generated by the three systems, under normal operating conditions, is due to the "quantization" process. This was corroborated by computing the noise power (N^2) at three different sampling rates. It was found that, for a fixed bandwidth f_c of the output filter, the product $N^2 f_p^3$ is approximately constant.

Input level		Cut-off frequencies HZ				% Improvements in bandwidths				
		LDM system	CVSD systems			HC-55516 w.r.t. LDM	MC-3417 w.r.t.		MC-3418 w.r.t.	
V_{p-p}	DB		HC-55516	MC-3417	MC-3418		LDM	HC-55516	LDM	HC-55516
4.0	0.0	260	600	2850	2250	130	996	375	765	275
2.0	-6.0	530	1050	3300	2450	98	523	214	362	133
1.0	-12.0	1070	1600	3400	2500	49.5	218	113	134	56
0.5	-18.0	2200	2200	3450	2700	0.0	57	57	23	23

Fig. 7-1 - Percentage improvement in bandwidths using syllabically companded systems (Motorola and Harris CVSD devices).

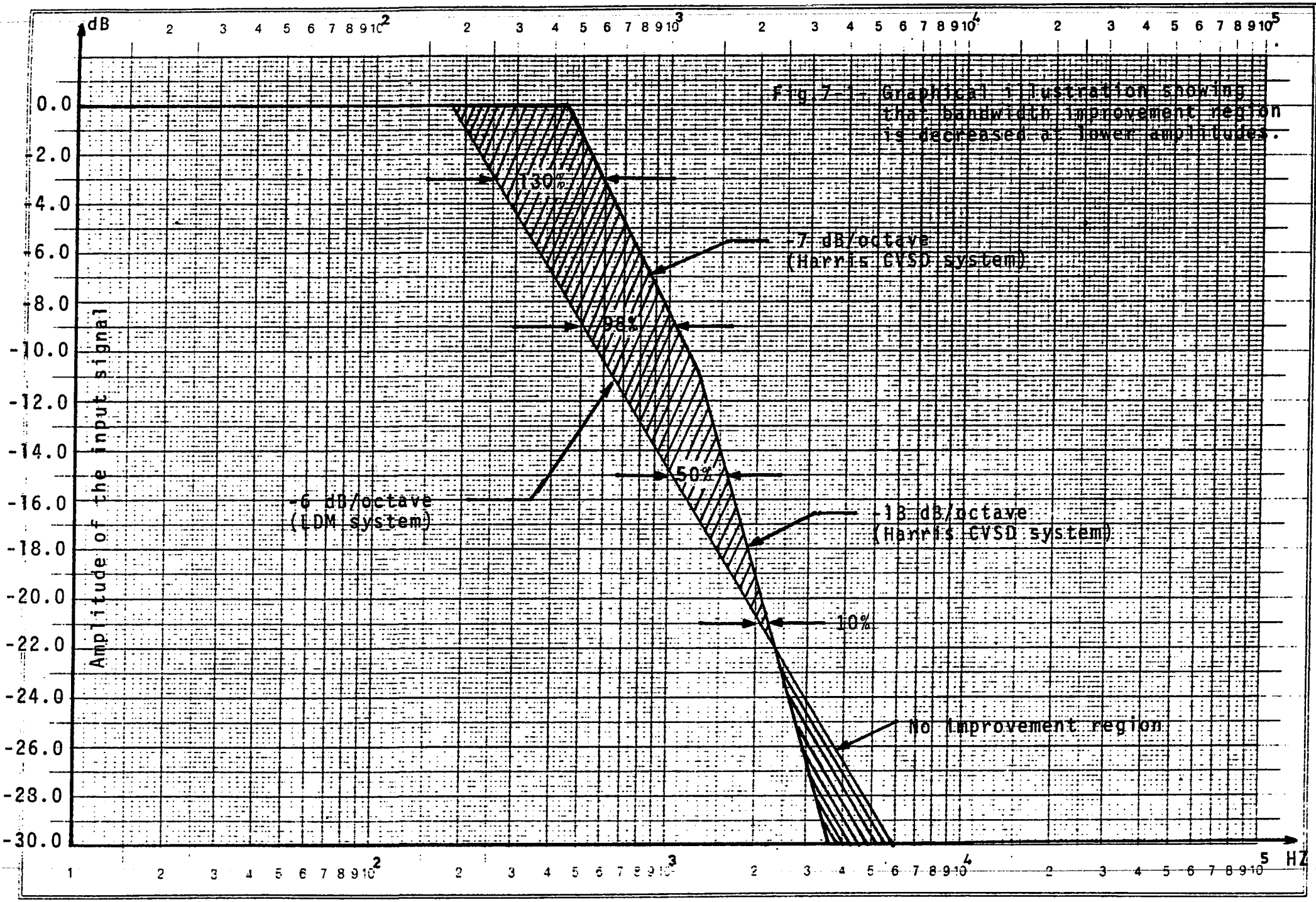

Fig 7-1. Graphical illustration showing that bandwidth improvement region is decreased at lower amplitudes.

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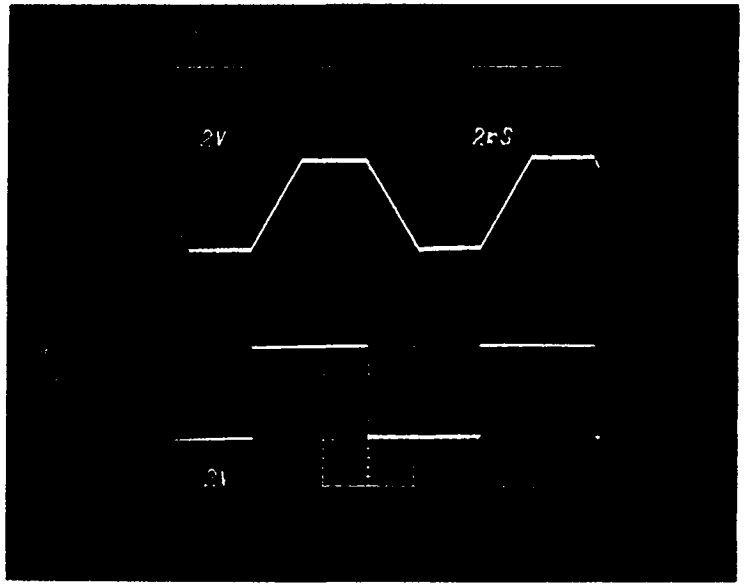
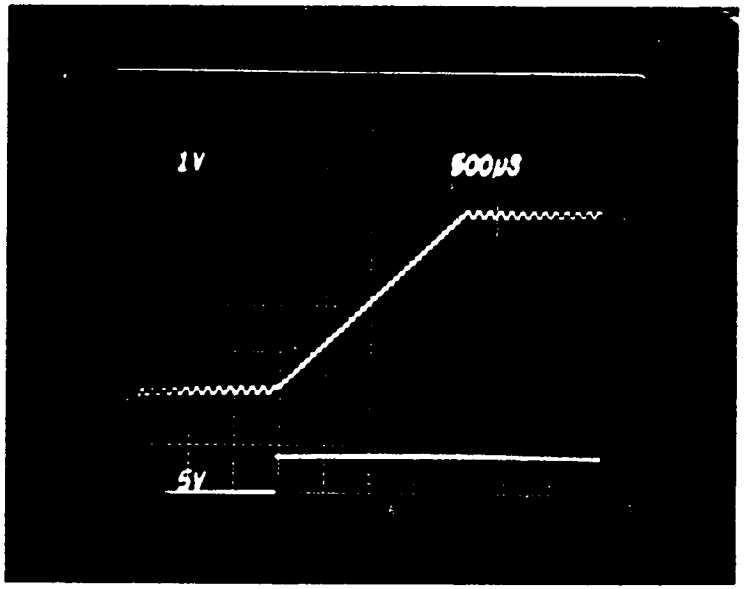
Step responses of the DM systems also provide performance measures. By comparing the response of the three tested systems (LDM, Harris and Motorola CVSD systems), with a low frequency square wave, (figures 7-2, 7-3 and 7-4) it is concluded that, companding using the Motorola device is much faster than the Harris device. The comparison shows that, the time required for the decoded signal to reach the newly switched level of the input step differs from one system to another. It is approximately 2.0 msec with the LDM system and approximately 1.4 msec with the Harris CVSD system. The Motorola CVSD system shows that the MC-3417 device is able to make this change at an approximate time of 0.58 msec whereas the MC-3418 device requires slightly longer time; i.e. approximately 0.64 msec (figure 7-5).

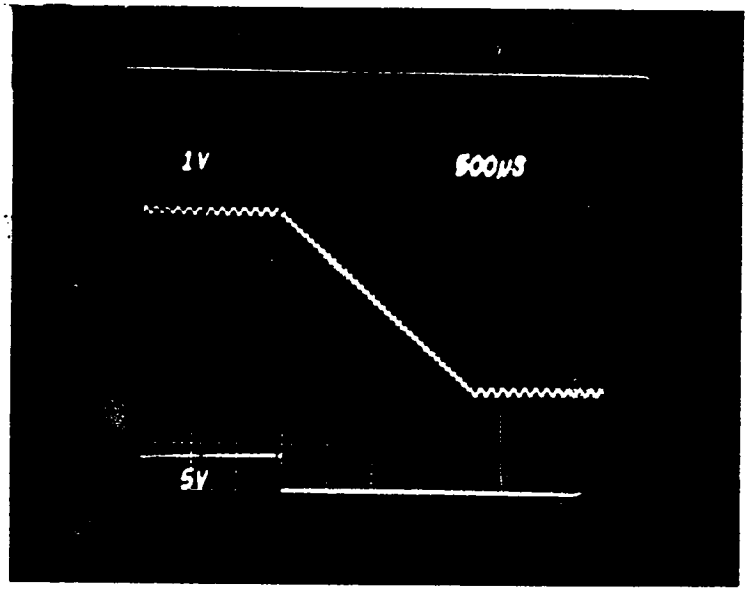
Although the Harris CVSD system needs very few external components and looks much simpler than a Motorola CVSD system, the latter system is usually more practical. This is because the performance of the Harris CVSD system depends upon the response of its internal predesigned (by the manufacturer) digital circuitry. There is no opportunity to alter the resulting performance of the system. A CVSD system using Motorola devices provides flexibility not existing for the Harris device. Examples of



a) Step response.

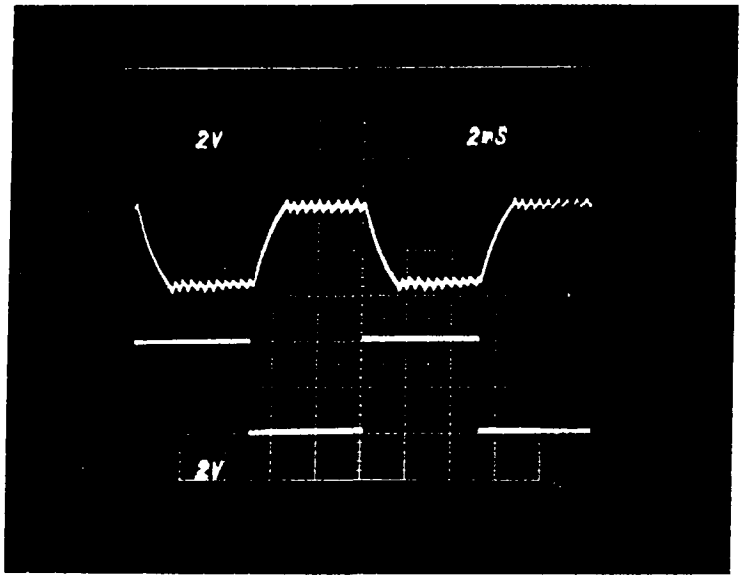


b) Rising portion of the step response.

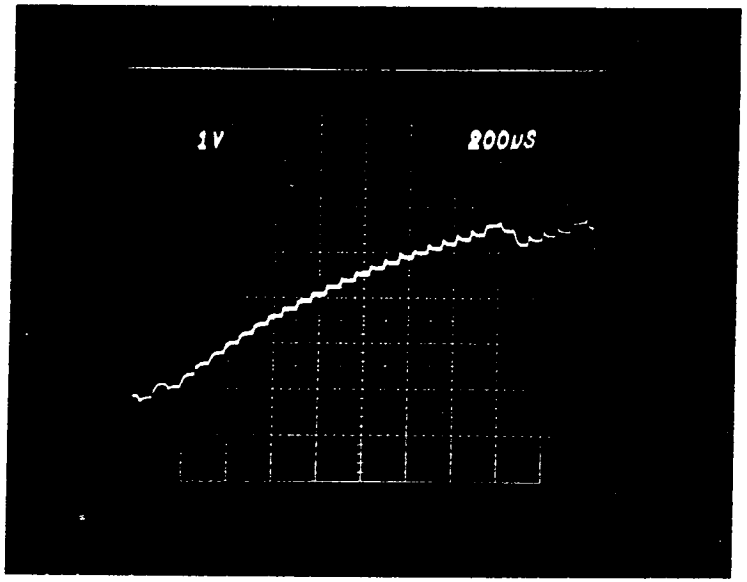


c) Falling portion of the step response.

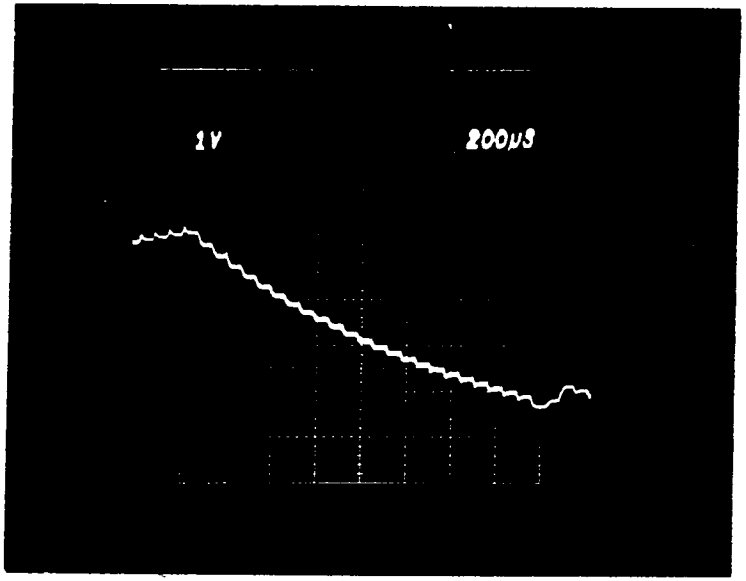
Fig.7-2 - Step response of the LDM system.
(Input condition 4.0V p-p at 100 HZ).



a) Step response.

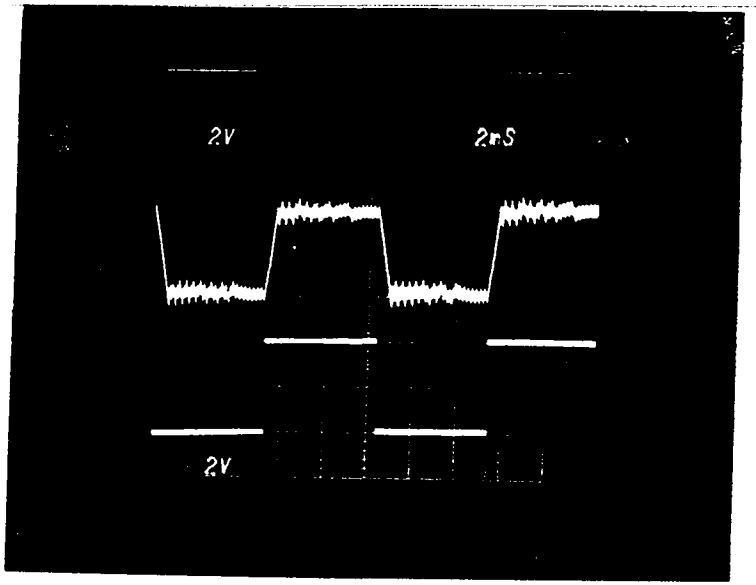


b) Rising portion of the step response.

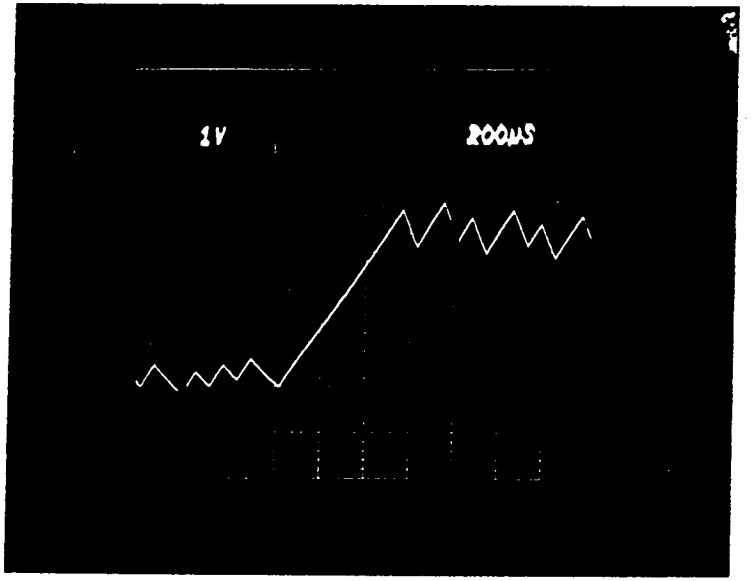


c) Falling portion of the step response.

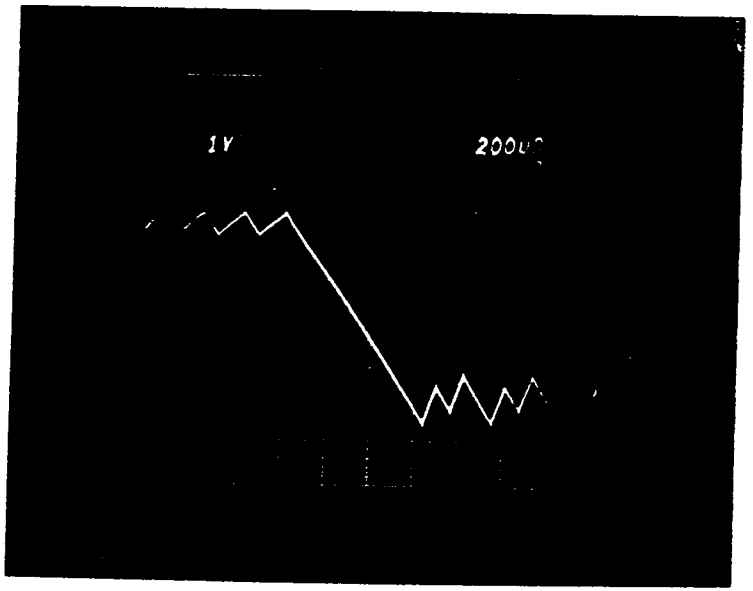
Fig. 7-3 - Step response of the Harris CVSD system (Input condition 4.0V_{p-p} at 100 HZ).



a) Step response

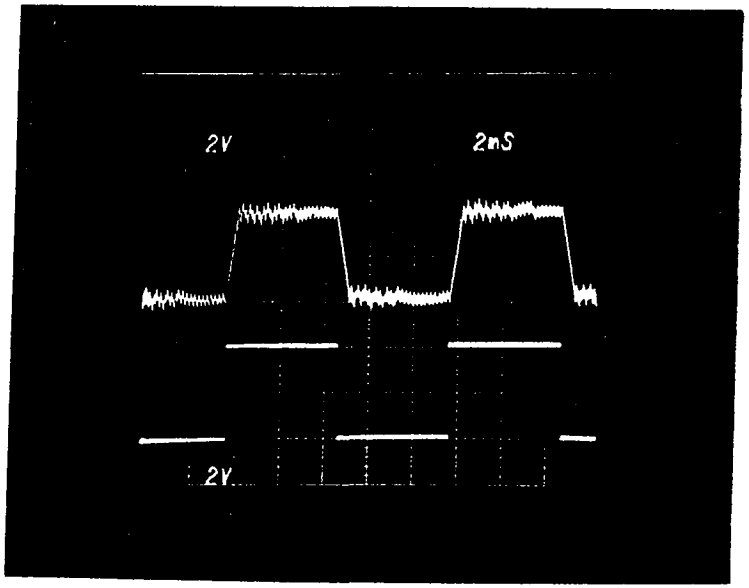


b) Rising portion of the step response

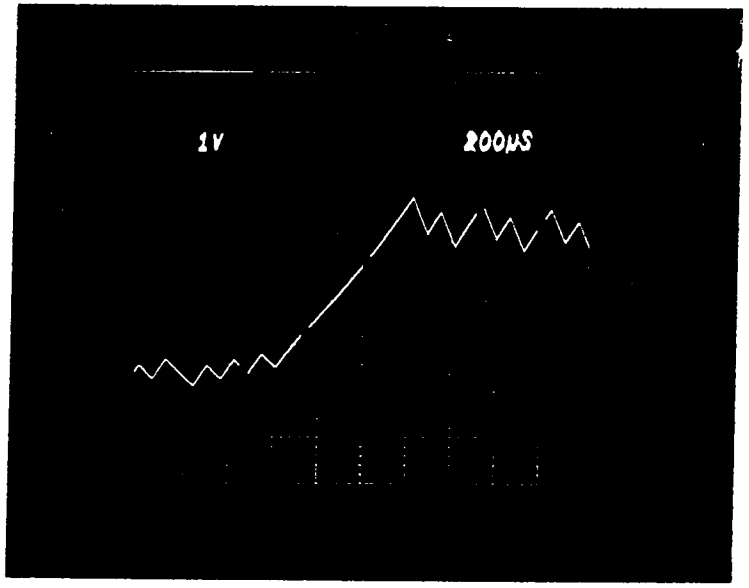


c) Falling portion of the step response.

Fig.7-4 - Step response of the Motorola (MC-3417) CVSD system (Input condition 4.0V p-p at 100 HZ).

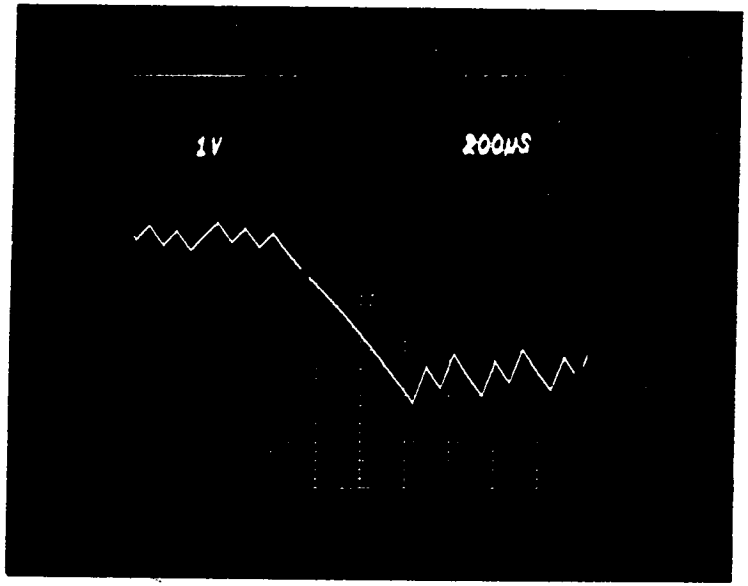


a) Step response.



b) Rising portion of the step response.

Fig.7-5 - Step response of the Motorola (MC-3418) CVSD system.(Input condition 4.0V p-p at 100 HZ).



c) Falling portion of the step response.

such flexibility are:

1- Possibility of adjusting the performance to meet a certain input condition. This can be accomplished by controlling the syllabic filter time constant and the loop gain of the system. Parameters which control the loop gain are, the idling pattern $|V_{cs}(Min)|$, integrating current ($I_{int} \propto \frac{1}{R_x}$) and the gain and the time constant of the integrator.

2- Possibility of varying the bandwidth of the system by choosing different shift register lengths in the SSA algorithm.

3- Possibility of varying the dynamic range of the system (Maximum amplitude of the input signal) by choosing different values for V_{cc} from 4.5V to 18.0V (see appendix-6).

4- For a prescribed dynamic range and shift register length, it is possible to control the bandwidth of the system by changing the sampling rate f_p. Higher sampling rates provide wider bandwidths.

7-2 Future Work

The preceding work describes the performance of the CVSD systems built as integrated circuit chips. Single pole filters were used to obtain the companded feedback signal.

However, by making these filters more complicate; e.g. a double pole syllabic filter and/or using double integration to determine the feedback signal, system performance can be improved. The decoded signal for idling, and for slope overloading will differ from a simple ramp. It will have a more complicate form. Under normal operating conditions the error; i.e. quantization noise, will diminish. This leads to higher signal-to-noise ratios. Bandwidths and the "roll-off" will also be affected. It is suggested as future work to study various feedback filters (both linear and nonlinear) to determine design guidelines for performance requirements.

The Harris device (HC-55516/HC-55532) uses a completely digital circuit in its feedback loop. The performance of the CVSD system using such device was found to be dependent upon the internal design of the device. The filters were indicated to be single pole, recursive. No information was given about the type of digital pattern at the input of the 10-bit DAC. As future work, to improve the performance of Harris device, it is recommended to computer simulate digital network which functions as the Harris device. The single pole recursive digital filter and the entire digital approach may, from the simulation results, lead to an improved design or suggest external

circuitry for accomplishing this. As a trial, the principle of delta sigma modulation (DSM) system can be used to improve the performance of the Harris device. This can be accomplished by applying the integration of the input analogue signal to the input of the Harris device.

Applications of CVSD chips in fields other than speech encoding can be studied as future work. Transfer function characteristics for the Motorola and the Harris chips (figures 5-20 and 6-25) suggest an application as low-pass filters. The Harris device can be used to provide a low-pass filter at approximately -12 dB/octave. Motorola devices can be used to achieve very steep attenuation above the cut-off frequencies. Both the Motorola and the Harris devices provide low-pass filters whose bandwidths can be controlled just by changing the sampling rate of the system. Other potential applications can also be studied.

Appendix -.1

Fourier Series Expansion

In this appendix Fourier series expansions of several periodic waveforms applicable to the idling condition of the LDM system (Chapter-3) and of the Harris (CVSD) system (Chapter-6) are discussed. The trapezoidal wave was common for both systems, its assymmetric form was analyzed first for the Fourier series co-efficients a_o, a_n and b_n, and then those co-efficients were simplified to match the form mentioned in Chapters 3 and 6.

Fourier series expansion of a bounded periodic function f(x) is given by |18|:

$$f(x) = \frac{a_o}{2} + \sum_{n=1}^{\infty} \left(a_n \operatorname{Cos} \frac{n\pi}{L} x + b_n \operatorname{Sin} \frac{n\pi}{L} x\right) \qquad \text{(A1-1)}$$

Where: a_o, a_n and b_n are the Fourier series co-efficients and are given by:

$$a_o = \frac{1}{L} \int_{-L}^{L} f(x)\, dx \qquad \text{(A1-2)}$$

$$a_n = \frac{1}{L} \int_{-L}^{L} f(x) \operatorname{Cos} \frac{n\pi}{L} x\, dx \qquad \text{(A1-3)}$$

$$b_n = \frac{1}{L} \int_{-L}^{L} f(x) \operatorname{Sin} \frac{n\pi}{L} x\, dx \qquad \text{(A1-4)}$$

Where: L is half the period of the periodic function f(x).

In cosine form the Fourier expansion of f(x) is [18]:

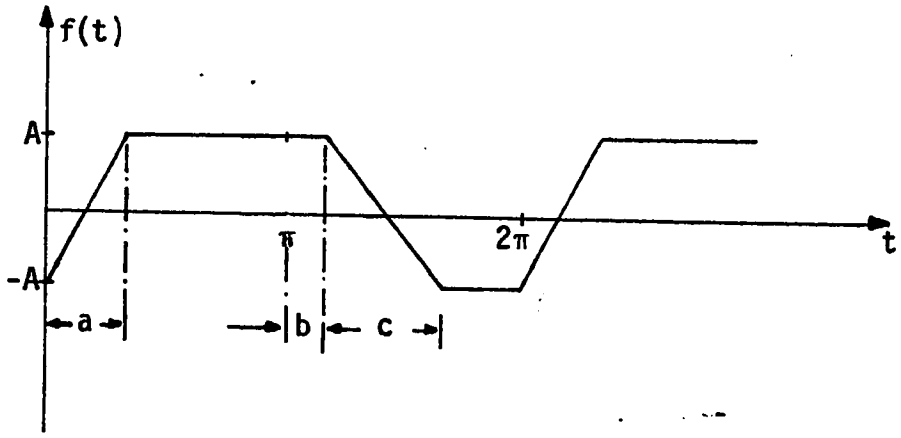
$$f(x) = \frac{a_o}{2} + \sum_{n=1}^{\infty} C_n \cos\left(\frac{n\pi}{L} x + \phi_n\right) \qquad \text{(A1-5)}$$

where $C_n = \sqrt{a_n^2 + b_n^2}$ and $\phi_n = \tan^{-1} \frac{a_n}{b_n}$

A1-1 Trapezoidal wave

Considering an assymmetric form of the trapezoidal wave as shown in figure A1-1, the Fourier series co-efficients a_o, a_n and b_n are:

$$a_o = \frac{A}{\pi} (2b + c - a) \qquad \text{(A1-6)}$$



$a \neq c$ and $b > o$

$$f(t) \begin{cases} = \frac{2A}{a} t - A & o \leq t \leq a \\ = A & a \leq t \leq \pi + b \\ = -\frac{2A}{c} t + 2A \frac{(\pi+b)}{c} + A & \pi + b \leq t \leq (\pi+b) + c \\ = -A & (\pi+b) + c \leq t \leq 2\pi \end{cases}$$

Fig. A1-1 - Assymmetrical Trapezoidal waveform; i.e. $a \neq c$ and $b > o$.

$$a_n = \frac{2A}{n^2\pi}\left[\frac{1}{a}(\text{Cos na} + \frac{na}{2}\text{Sin na} - 1) - \frac{1}{c}\text{Cos } n\pi\left\{\text{Cos n(b+c)}\right.\right.$$

$$\left.\left. + \frac{nc}{2}\overline{\text{Sin n(b+c) + Sin nb}} - \text{Cos nb}\right\}\right] +$$

$$\frac{A}{n\pi}\left[\text{Cos } n\pi\left\{\text{Sin nb + Sin n(b+c)}\right\} - \text{Sin na}\right] \qquad \text{(A1-7)}$$

$$b_n = \frac{2A}{n^2\pi}\left[\frac{1}{a}\left\{\text{Sin na} - \frac{na}{2}(\text{Cos na} + 1)\right\} - \frac{1}{c}\text{Cos } n\pi\left\{\text{Sin n(b+c)}\right.\right.$$

$$\left.\left. - \frac{nc}{2}\overline{\text{Cos n(b+c) + Cos nb}} - \text{Sin nb}\right\}\right] - \frac{A}{n\pi}\left[\text{Cos } n\pi\left\{\text{Cos nb}\right.\right.$$

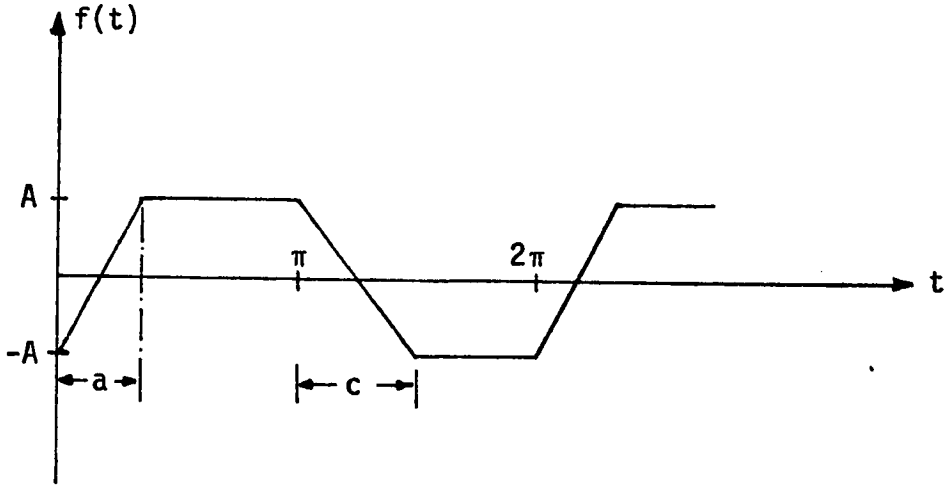
$$\left.\left. + \text{Cos n(b+c)}\right\} - (\text{Cos na} + 1)\right] \qquad \text{(A1-8)}$$

A1-2 Special forms of the trapezoidal waveform

In this section the Fourier series co-efficients given by equations (A1-6), (A1-7), and (A1-8) are simplified to correspond the waveforms mentioned in Chapters 3 and 6.

A1-2.1 Assymmetric trapezoidal wave with a ≠ c and b = o

This form of the trapezoidal wave is shown in figure A1-2. It is the approximate sketch of the decoded wave under the idling condition of the LDM system (Chapter-3).



$a \neq c$

$$f(t) \begin{cases} = \frac{2A}{a} t - A & 0 \leq t \leq a \\ = A & a \leq t \leq \pi \\ = -\frac{2A}{a} t + 2A \frac{\pi}{c} + A & \pi \leq t \leq \pi + c \\ = -A & \pi + c \leq t \leq 2\pi \end{cases}$$

Fig. A1-2 - Trapezoidal wave having assymmetrical rising and falling time periods.

The Fourier series co-efficients are obtained just by putting b=o in equations (A1-6), (A1-7), and (A1-8). Then these co-efficients are:

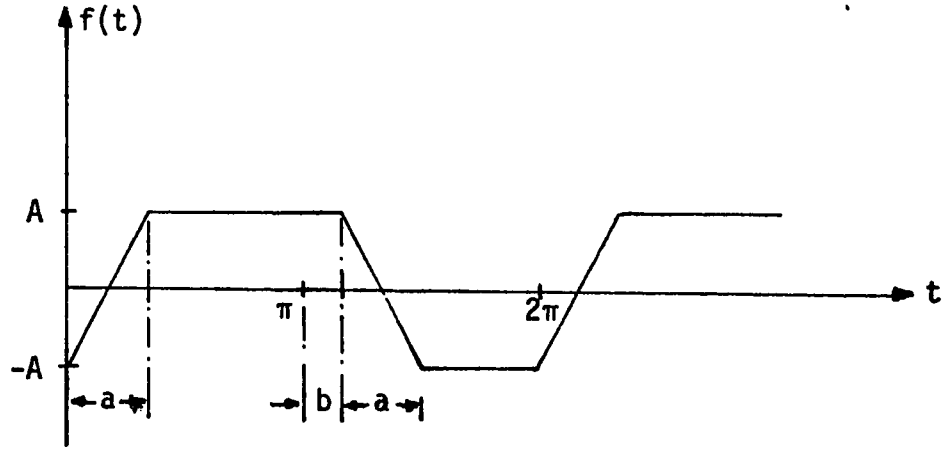
$$a_o = \frac{A}{\pi} (c - a) \qquad \text{(A1-9)}$$

$$a_n = \frac{2A}{n^2\pi}\left[\frac{1}{a}\left(\text{Cos na} + \frac{na}{2}\text{ Sin a} - 1\right) - \frac{1}{c}\text{ Cos n}\pi\left\{\text{Cos nc} + \frac{nc}{2}\text{ Sin nc} - 1\right\}\right] + \frac{A}{n\pi}\left[\text{Cos n}\pi\text{ Sin nc} - \text{Sin na}\right] \qquad \text{(A1-10)}$$

$$b_n = \frac{2A}{n^2\pi}\left[\frac{1}{a}\left\{\text{Sin na} - \frac{na}{2}\left(\text{Cos na} + 1\right)\right\} - \frac{1}{c}\text{ Cos n}\pi\left\{\text{Sin nc} - \frac{nc}{2}\left(\text{Cos nc} + 1\right)\right\}\right] - \frac{A}{n\pi}\left[\text{Cos n}\pi(1 + \text{Cos nc}) - (\text{Cos na} + 1)\right] \qquad \text{(A1-11)}$$

A1-2.2 - Assymmetric trapezoidal with a=c and b>o

This form of the trapezoidal wave is shown in figure A1-3. It is a part of the decoded wave under idling condition of the Harris (CVSD) modulation system (Chapter-6).



$$f(t) \begin{cases} = \frac{2A}{a} t - A & 0 \leq t \leq a \\ = A & a \leq t \leq \pi + b \\ = -\frac{2A}{a} + 2\pi \frac{(\pi+b)}{a} + A & (\pi+b) \leq t \leq (\pi+b) + a \\ = -A & (\pi+b) + a \leq t \leq 2\pi \end{cases}$$

Fig. A1-3 - Trapezoidal wave having symmetrical rising and falling time periods but unequal time periods for the positive and the negative constant levels.

The Fourier series co-efficients are obtained by putting a=c in equations (A1-6), (A1-7), and (A1-8). Then these co-efficients are:

$$a_o = \frac{2Ab}{\pi} \qquad \text{(A1-12)}$$

$$a_n = \frac{2A}{n^2\pi}\left[\frac{1}{a}(\text{Cos } na + \frac{na}{2}\text{ Sin } na - 1) - \frac{1}{a}\text{Cos } n\pi\left\{\text{Cos } n(b+a) + \frac{na}{2}\cdot\overline{\text{Sin } n(b+a) + \text{Sin } nb} - \text{Cos } nb\right\}\right] + \frac{A}{n\pi}\left[\text{Cos } n\pi\left\{\text{Sin } nb + \text{Sin } n(b+a)\right\} - \text{Sin } na\right] \quad \text{(A1-13)}$$

$$b_n = \frac{2A}{n^2\pi}\left[\frac{1}{a}\left\{\text{Sin } na - \frac{na}{2}(\text{Cos } na + 1)\right\} - \frac{1}{a}\text{Cos } n\pi\left\{\text{Sin } n(b+a) - \frac{na}{2}\cdot\overline{\text{Cos } n(b+a) + \text{Cos } nb} - \text{Sin } nb\right\}\right] - \frac{A}{n\pi}\left[\text{Cos } n\pi\left\{\text{Cos } nb + \text{Cos } n(b+a)\right\} - (\text{Cos } na + 1)\right] \quad \text{(A1-14)}$$

A1-3 - The rampwise pulses

This wave consists of a train of pulses having a rampwise rising and falling edges (figure A1-4). It is part of the decoded wave under the idling condition of the Harris (CVSD) modulation system (Chapter-6).

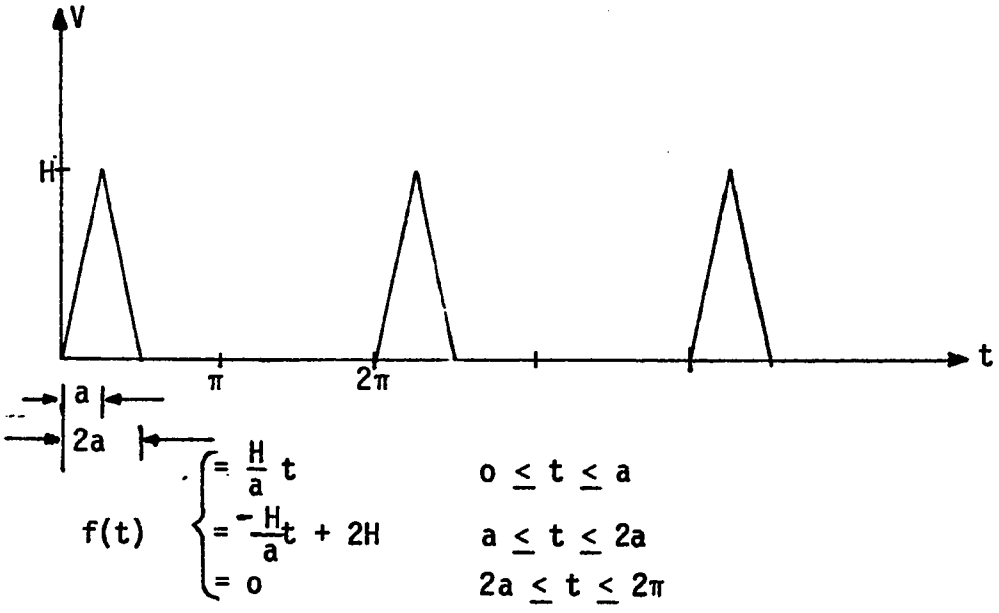


Fig. A1-4 - Rampwise train of pulses.

The Fourier series co-efficients for such a wave using equations (A1-2), (A1-3), and (A1-4) yields:

$$a_o = \frac{aH}{\pi} \qquad \text{(A1-15)}$$

$$a_n = \frac{H}{n^2 a\pi}\left[2\text{Cos } na - (\text{Cos } 2na + 1)\right] \qquad \text{(A1-16)}$$

$$b_n = \frac{H}{n^2 a\pi}\left[2\text{Sin } na - \text{Sin } 2na\right] \qquad \text{(A1-17)}$$

A1-4 - Computation of the Fourier co-efficients

In this section the peak value of the frequency spectrum (fundamental and its harmonics) of the decoded wave under idling condition for both LDM and Harris CVSD system are computed.

A1-4.1 - Linear delta modulation system

Using equations (A1-7), and (A1-8) the Fourier series co-efficients a_n and b_n are computed for different values of n. The constants A, a and c were obtained from figure 3-9., such that:

$A = 60$ mv

$a \simeq 0.192\pi \simeq 34.56^o$

$c \simeq 0.16\pi \simeq 38.8^o$

The peak value of the fundamental (n=1) and its harmonics upto n=6 are tabulated in table A1-1.

n	a_n	b_n	$C_n=\sqrt{a_n^2 + b_n^2}$	$\phi_n=\tan^{-1}\frac{a_n}{b_n}$	f_n KHZ
1	-20.57	72.54	75.40	-16^0	8.0
2	-1.38	-1.24	1.86	48^0	16.0
3	-16.61	15.26	22.56	-47^0	24.0
4	-0.14	-1.66	1.67	5^0	32.0
5	-10.54	2.10	10.75	-79^0	40.0
6	-0.09	1.07	1.078	-5^0	48.0

Table A1-1 - Computed peaks of the frequency spectrum of the LDM system's decoded wave under idling condition.

A1-4.2 - Harris CVSD modulation system

The approximate sketch of the decoded wave under idling condition (figure 6-4) assumes that the delaying period (b) in the trapezoidal wave shown in figure A1-3 is equal to the rising/falling period (a); i.e. b=a. Using this assumption equations (A1-12), (A1-13), and (A1-14) are further simplified to:

$$a_o = \frac{2A}{\pi} a \qquad \text{(A1-18)}$$

$$a_n = \frac{2A}{n^2\pi}\left[\frac{1}{a}(\text{Cos } 2na - 1)\right] \quad n = \text{odd} \qquad \text{(A1-19)}$$

$$a_n = \frac{2A}{n^2\pi}\left[\frac{1}{a}(2\text{Cos } na - (\text{Cos } 2na + 1)\right] \quad n=\text{even} \qquad \text{(A1-20)}$$

$$b_n = \frac{2A}{n^2\pi}\left(\frac{1}{a}\text{ Sin } 2na\right) \quad n = \text{odd} \qquad \text{(A1-21)}$$

$$b_n = \frac{2A}{n^2\pi}\left[\frac{1}{a}(2\text{Sin } na - \text{Sin } 2na)\right] \quad n=\text{even} \qquad \text{(A1-22)}$$

The co-efficients A and (a) for the trapezoidal wave were obtained from figure 6-4b such that:

$A = 7.0$ mv

$a \simeq 0.1\pi \simeq 18^o$

Substituting the values of A and a in equation A1-19, (A1-20), (A1-21), and (A1-22) the co-efficients a_n and b_n were computed for different values of n (table A1-2a).

Fourier series co-efficients a_n and b_n for the rampwise pulses (figure A1-4) were obtained (table A1-2b) using equations (A1-16), and (A1-17). The co-efficients (H) and (a) were obtained from figure 6-4b such that:

$H = 25$ mv

$a \simeq 0.2\pi \simeq 36.0^{o}$

The total resulting peaks of decoded wave under idling condition of the Harris CVSD system is the vector addition of the Fourier co-efficients a_n and b_n obtained for the trapezoidal and the rampwise waveforms. The peak value of the fundamental (n=1) and its harmonics upto n=6 are tabulated in table A4-2c.

a) Trapezoidal wave				b) Rampwise pulses				c) Total spectrum of the decoded wave					
n	a_n 10^{-3}	b_n 10^{-3}	f_n KHZ	n	a_n 10^{-3}	b_n 10^{-3}	f_n KHZ	n	a_n 10^{-3}	b_n 10^{-3}	$C_n=\sqrt{a_n^2+b_n^2}$ 10^{-3}	$\phi_n=\tan^{-1}\frac{a_n}{b_n}$	f_n KHZ
1	-2.71	7.00	8.0					1	-2.71	7.0	7.51	-21.2	8.0
2	1.10	0.79	16.0	1	3.92	3.23	16.0	2	5.02	4.02	6.43	51.3	16.0
3	-1.85	1.37	24.0					3	-1.85	1.37	2.30	-53.5	24.0
4	0.39	1.19	32.0	2	1.35	4.12	32.0	4	1.74	5.31	5.60	18.14	32.0
5	-1.13	-	40.0					5	-1.13	-	1.13	90.0	40.0
6	-0.32	0.98	48.0	3	-1.14	3.5	48.0	6	-1.46	4.48	4.71	-18.05	48.0

Table A1-2 - Peak values of the Fourier series expansion of the Harris CVSD system's under idling conditions.

APPENDIX - 2

Noise power computation using straight line approximation method

In this appendix the noise generated by the implemented LDM system in its normal operating condition is computed using straight line approximation method. Straight line approximation of the actual frequency spectrum of the locally decoded waveforms shown in figures 3-17, 3-18 and 3-19 results in a continuous distribution; i.e. according to a function A(f). The total energy content within a certain bandwidth f_c is then given by |17 |.

$$W = \int_{f_a}^{f_b} [A(f)]^2 \, df \qquad (A2\text{-}1)$$

Equation A2-1 represents the area formed by $|A(f)|^2$ and f_c.
The function A(f) composed of straight line segments defined by:

$$A(f) = mf + k \qquad (A2\text{-}2)$$

Where:m is the slope of the straight line and k is a constant.
By squaring A(f), the area within a band $(f_p - f_a)$ is:

$$A = \int_{f_b}^{f_a} (m^2f^2 + 2mkf + k^2) \, df$$

or

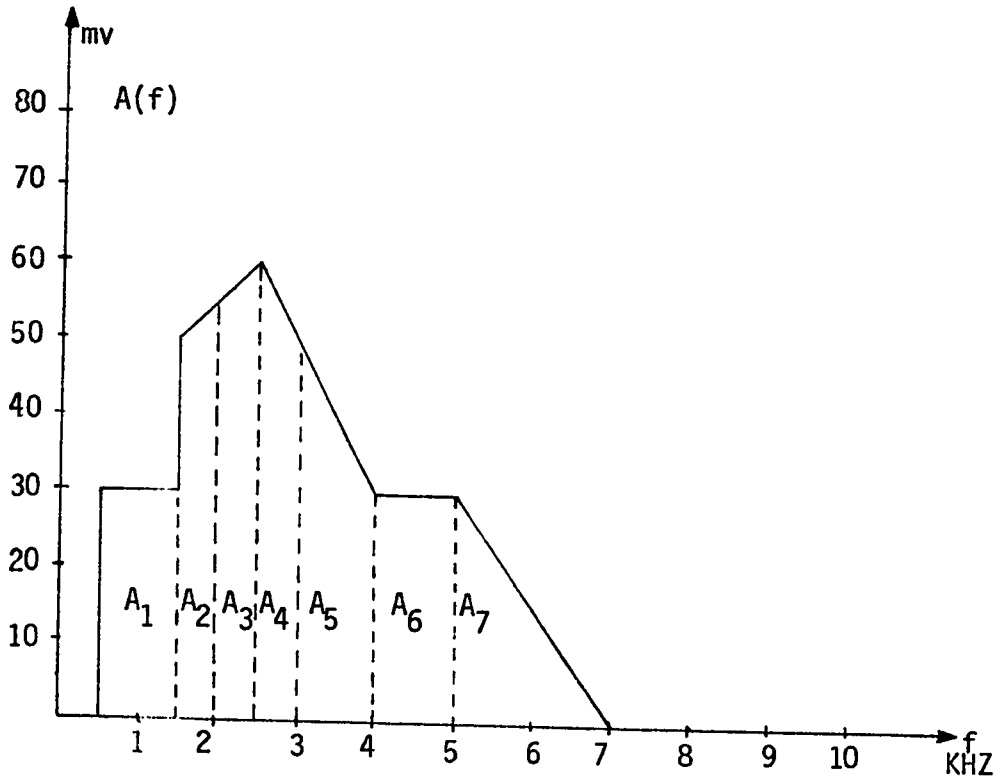
$$A = \left(\frac{1}{3} m^2f^3 + mkf^2 + kf\right)_{f_a}^{f_b} \qquad (A2\text{-}3)$$

The total energy is the summation of these areas; i.e.:

$$W_T = \sum_{n=1}^{\infty} A_n \qquad \text{(A2-4)}$$

Where:n is number of subdivided areas in a bandwidth f_c.

The straight line approximation of figures 3-17, 3-18 and 3-19 is shown in figures A2-1, A2-2 and A2-3, respectively. The area under each straight line section in those figures is obtained using equation A2-3. The computed areas, their summation to obtain W_T and the mean value of W_T for different selected bandwidths for each figure (A2-1, A2-2 and A2-3) are tabulated in tables A2-1, A2-2 and A2-3, respectively.

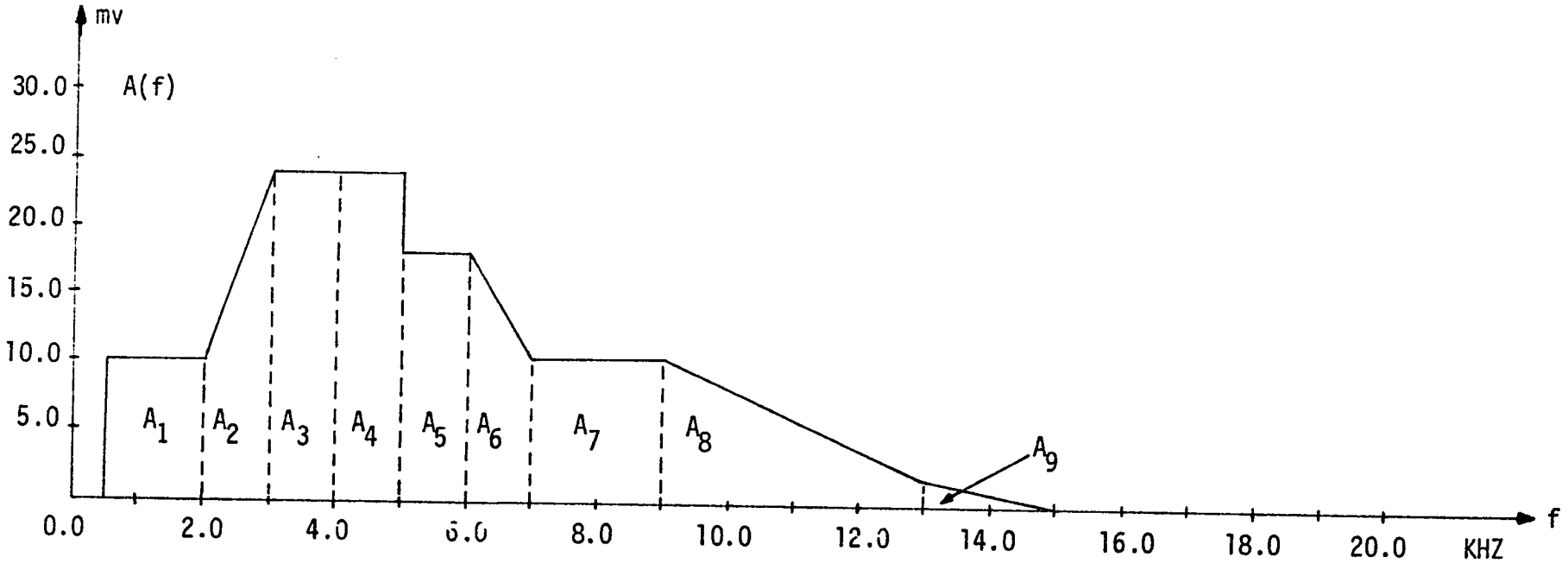


$$A(f) \begin{cases} = 30 \text{ mv} & 0.5 \leq f \leq 1.5 \text{ KHZ} \\ = (0.01f + 35) \text{ mv} & 1.5 \leq f \leq 2.5 \text{ KHZ} \\ = (-0.02\ f + 110) \text{mv} & 2.5 \leq f \leq 4.0 \text{ KHZ} \\ = 30 \text{ mv} & 4.0 \leq f \leq 5.0 \text{ KHZ} \\ = (-0.015\ f + 105) \text{mv} & 5.0 \leq f \leq 7.0 \text{ KHZ} \end{cases}$$

Fig. A2-1 - Straight line approximate of figure 3-17.

Bandwidth f_c KHZ	A_1 0.5-1.5 KHZ	A_2 1.5-2.0 KHZ	A_3 2.0-2.5 KHZ	A_4 2.5-3.0 KHZ	A_5 3.0-4.0 KHZ	A_6 4.0-5.0 KHZ	A_7 5.0-7.0 KHZ	$A_T = \sum_{n=1}^{\infty} A_n$ $V^2 f$	$W_{av} = \frac{A_T}{f_c} \frac{V^2}{V^2}$
0.5 - 3.0	0.9	1.376	1.654	1.517	-	-	-	5.447	2179×10^{-6}
0.5 - 4.0	0.9	1.376	1.654	1.517	1.633	-	-	7.08	2023×10^{-6}
0.5 - 5.0	0.9	1.376	1.654	1.517	1.633	0.9	-	7.98	1773×10^{-6}
0.5 - 7.0	0.9	1.376	1.654	1.517	1.633	0.9	0.6	8.58	1320×10^{-6}
2.0 - 5.0	-	-	1.654	1.517	1.633	0.9	-	5.704	1901×10^{-6}

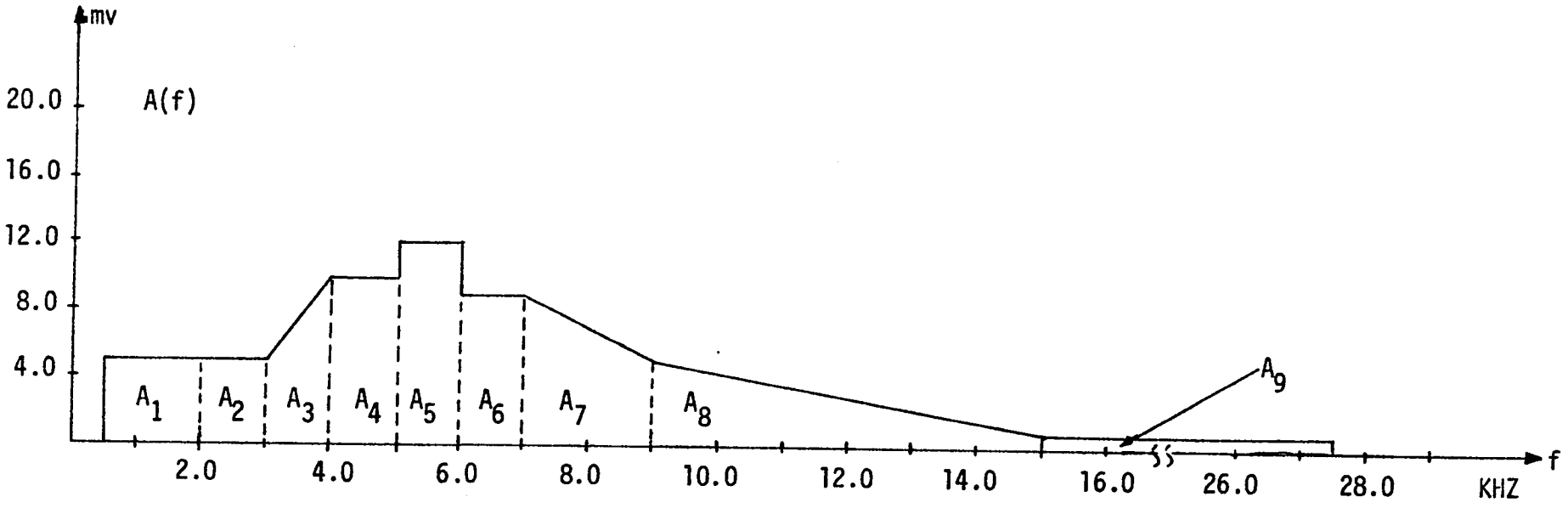
Table A2-1 - Computed average energies distribution.
Choosing different bandwidths f_c at the output.
Sampling rate f_p = 8.0 KHZ



$$A(f) \begin{cases} = 10 \text{ mv} & 0.5 \leq f \leq 2.0 \text{ KHZ} \\ = (14\times10^{-3} f - 18.0) \text{ mv} & 2.0 \leq f \leq 3.0 \text{ KHZ} \\ = 24.0 \text{ mv} & 3.0 \leq f \leq 5.0 \text{ KHZ} \\ = 18.0 \text{ mv} & 5.0 \leq f \leq 6.0 \text{ KHZ} \\ = (-8\times10^{-3} f + 66.0) \text{ mv} & 6.0 \leq f \leq 7.0 \text{ KHZ} \\ = 10.0 \text{ mv} & 7.0 \leq f \leq 9.0 \text{ KHZ} \\ = (-2\times10^{-3} f + 28) \text{ mv} & 9.0 \leq f \leq 13.0 \text{ KHZ} \\ = (-10^{-3} f + 15) \text{ mv} & 13.0 \leq f \leq 15.0 \text{ KHZ} \end{cases}$$

Bandwidth f_c KHZ	A_1 0.5-2.0 KHZ	A_2 2.0-3.0 KHZ	A_3 3.0-4.0 KHZ	A_4 4.0-5.0 KHZ	A_5 5.0-6.0 KHZ	A_6 6.0-7.0 KHZ	A_7 7.0-9.0 KHZ	A_8 9.0-13.0 KHZ	A_9 13.0-15.0 KHZ	$A_T = \sum_{n=1}^{9} A_n$ $V^2 f$	$W_{av} = \frac{A_T}{f_c}$ V^2
0.5 - 3.0	0.15	0.035	-	-	-	-	-	-	-	0.455	182×10^{-6}
0.5 - 4.0	0.15	0.305	0.576	-	-	-	-	-	-	1.031	295×10^{-6}
0.5 - 5.0	0.15	0.305	0.576	0.576	-	-	-	-	-	1.607	357×10^{-6}
0.5 - 15.0	0.15	0.305	0.576	0.576	0.324	0.201	0.200	0.165	0.003	2.500	172×10^{-6}
2.0 - 5.0	-	0.305	0.576	0.576	-	-	-	-	-	1.457	486×10^{-6}

Table A2-2 - Computed average energies distribution, choosing different bandwidths at the output. Sampling rate f_p = 16.0 KHZ.



$$A(f) \begin{cases} = 5.0 \text{ mv} & 0.5 \leq f \leq 3.0 \text{ KHZ} \\ = (5.0 \times 10^{-3} f - 100) \text{ mv} & 3.0 \leq f \leq 4.0 \text{ KHZ} \\ = 10.0 \text{ mv} & 4.0 \leq f \leq 5.0 \text{ KHZ} \\ = 12.0 \text{ mv} & 5.0 \leq f \leq 6.0 \text{ KHZ} \\ = 9.0 \text{ mv} & 6.0 \leq f \leq 7.0 \text{ KHZ} \\ = (-2.5 \times 10^{-3} f + 26.5) \text{ mv} & 7.0 \leq f \leq 9.0 \text{ KHZ} \\ = (-0.5 \times 10^{-3} f + 8.5) \text{ mv} & 9.0 \leq f \leq 15.0 \text{ KHZ} \\ = 1.0 \text{ mv} & 15.0 \leq f \leq 27.5 \text{ KHZ} \end{cases}$$

Bandwidth f_c KHZ	A_1 0.5-2.0 KHZ	A_2 2.0-3.0 KHZ	A_3 3.0-4.0 KHZ	A_4 4.0-5.0 KHZ	A_5 5.0-6.0 KHZ	A_6 6.0-7.0 KHZ	A_7 7.0-9.0 KHZ	A_8 9.0-15.0 KHZ	A_9 15.0-27.5 KHZ	$A_T = \sum_{n=1}^{\infty} A_n$ $V^2 f$	$W_{av} = \frac{A_T}{f_c}$ V^2
0.5 - 3.0	0.0375	0.025	-	-	-	-	-	-	-	0.0625	25×10^{-6}
0.5 - 4.0	0.0375	0.025	0.058	-	-	-	-	-	-	0.1205	34×10^{-6}
0.5 - 5.0	0.0375	0.025	0.058	0.1	-	-	-	-	-	0.2205	49×10^{-6}
0.5 -27.5	0.0375	0.025	0.058	0.1	0.144	0.081	0.088	0.042	0.0125	0.588	22×10^{-6}
2.0 - 5.0	-	0.025	0.058	0.1	-	-	-	-	-	0.183	61×10^{-6}

Table A2-3 - Computed average energies distribution.
Choosing different bandwidths f_c at the output.
Sampling rate f_p = 32.0 KHZ

APPENDIX - 3

Absolute Maximum Ratings and Electrical Characteristics of Motorola and Harris Devices.

This appendix describes both the Motorola and the Harris devices in more details from the point of view of their absolute maximum ratings and electrical characteristics.

A3-1- Motorola Devices (MC3417/MC3517 or MC3418/MC3518)

The complete schematic diagram of the internal parts of the Motorola devices (MC3417/MC3517 and MC3418/MC3518) is shown in figure A6-1. The absolute maximum ratings and electrical characteristics are given in Tables A3-1 and A3-2, respectively.

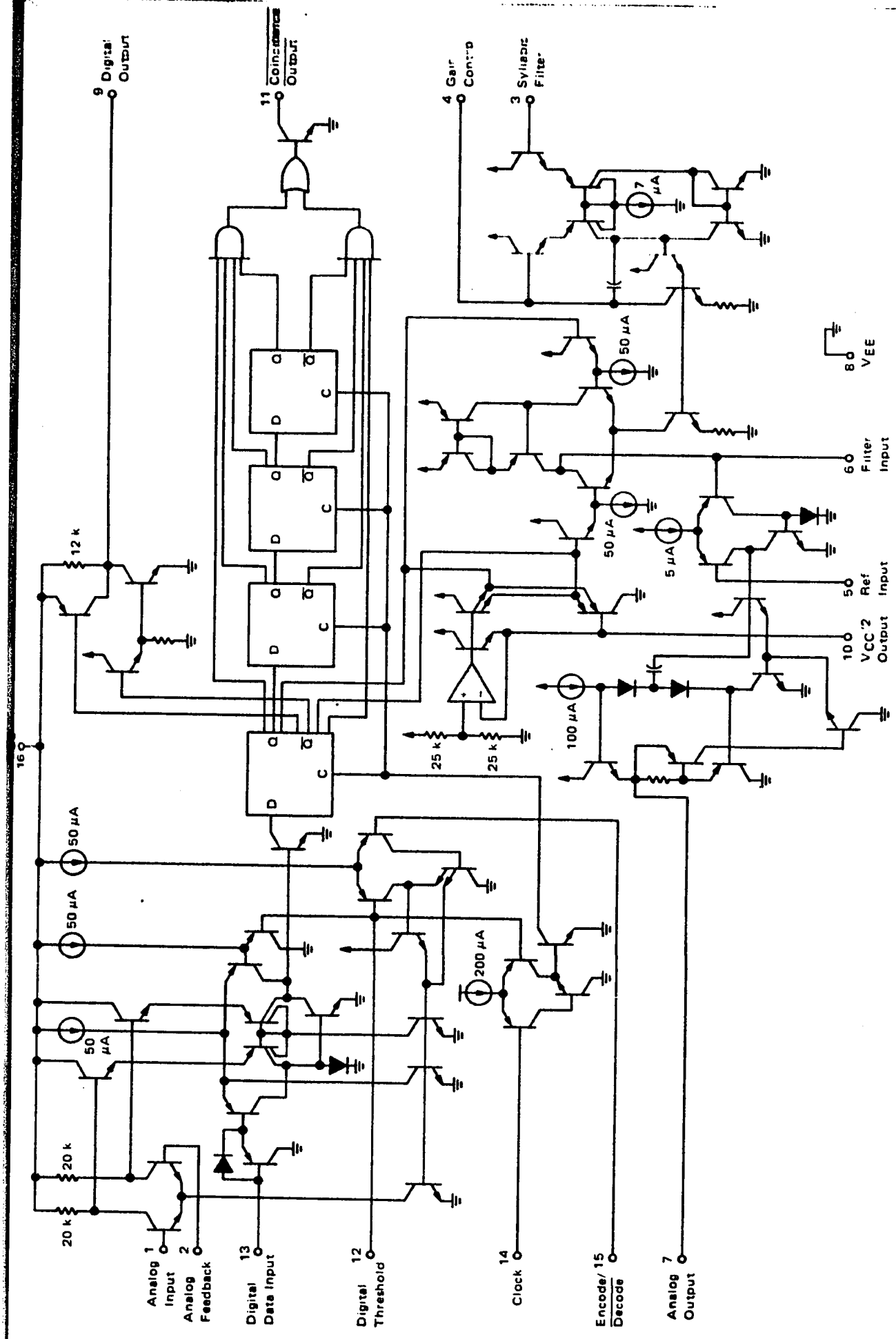


Fig. A.3-1 - Schematic diagram of Motorola CVSD system MC3417/MC3517 and MC3418/MC3518.

MAXIMUM RATINGS

(All voltages referenced to V_{EE}, T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	$V_{CC}/2$ − 1.0 to V_{CC}	Vdc
$V_{CC}/2$ Output Current	I_{Ref}	−25	mA

Table A3-1

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0°C to +70°C for MC3417/18, T_A = −55°C to +125°C for MC3517/18 unless otherwise noted.)

Characteristic	Symbol	MC3417/MC3517			MC3418/MC3518			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range	V_{CCR}	4.75	12	16.5	4.75	12	16.5	Vdc
Power Supply Current (Idle Channel)	I_{CC}							mA
(V_{CC} = 5.0 V)		–	3.7	5.0	–	3.7	5.0	
(V_{CC} = 15 V)		–	6.0	10	–	6.0	10	
Clock Rate	SR	–	16 k	–	–	32 k	–	Samples/s
Gain Control Current Range	I_{GCR}	0.001	–	3.0	0.001	–	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) (4.75 V ≤ V_{CC} ≤ 16.5 V)	V_I	1.3	–	V_{CC} − 1.3	1.3	–	V_{CC} − 1.3	Vdc
Analog Output Range (Pin 7) (4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ± 5.0 mA)	V_O	1.3	–	V_{CC} − 1.3	1.3	–	V_{CC} − 1.3	Vdc
Input Bias Currents (Comparator in Active Region)	I_{IB}							μA
Analog Input (I1)		–	0.5	1.5	–	0.25	1.0	
Analog Feedback (I2)		–	0.5	1.5	–	0.25	1.0	
Syllabic Filter Input (I3)		–	0.06	0.5	–	0.06	0.3	
Reference Input (I5)		–	−0.06	−0.5	–	−0.06	−0.3	
Input Offset Current (Comparator in Active Region)	I_{IO}							μA
Analog Input/Analog Feedback |I1 − I2|		–	0.15	0.6	–	0.05	0.4	
Integrator Amplifier |I5 − I6|		–	0.02	0.2	–	0.01	0.1	
Input Offset Voltages V/I Converter (Pins 3 and 4)	V_{IO}	–	2.0	6.0	–	2.0	6.0	mV
Transconductance	gm							mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	–	0.1	0.3	–	
Integrator Amplifier, 0 to ± 5.0 mA Load		1.0	10	–	1.0	10	–	
Propagation Delay Times (Note 1)								μs
Clock Trigger to Digital Output (C_L = 25 pF to Gnd)	t_{PLH}	–	1.0	2.5	–	1.0	2.5	
	t_{PHL}	–	0.8	2.5	–	0.8	2.5	
Clock Trigger to Coincidence Output (C_L = 25 pF to Gnd) (R_L = 4 kΩ to V_{CC})	t_{PLH}	–	1.0	3.0	–	1.0	3.0	
	t_{PHL}	–	0.8	2.0	–	0.8	2.0	
Coincidence Output Voltage — Low Logic State ($I_{OL(Con)}$ = 3.0 mA)	$V_{OL(Con)}$	–	0.12	0.25	–	0.12	0.25	Vdc
Coincidence Output Leakage Current — High Logic State (V_{OH} = 15.0 V, 0°C ≤ T_A ≤ 70°C)	$I_{OH(Con)}$	–	0.01	0.5	–	0.01	0.5	μA

NOTE 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	MC3417/MC3517 Min	MC3417/MC3517 Typ	MC3417/MC3517 Max	MC3418/MC3518 Min	MC3418/MC3518 Typ	MC3418/MC3518 Max	Unit
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	–	V_{CC} – 2.0	+1.2	–	V_{CC} – 2.0	Vdc
Digital Threshold Input Current ($1.2\ V \le V_{th} \le V_{CC} - 2.0\ V$)	$I_{I(th)}$							μA
(V_{IL} applied to Pins 13, 14 and 15)		–	–	5.0	–	–	5.0	
(V_{IH} applied to Pins 13, 14 and 15)		–	-10	-50	–	-10	-50	
Maximum Integrator Amplifier Output Current	I_O	±5.0		-	±5.0			mA
$V_{CC}/2$ Generator Maximum Output Current (Source only)	I_{Ref}	+10			+10			mA
$V_{CC}/2$ Generator Output Impedance (0 to +10 mA)	z_{Ref}	–	3.0	6.0	–	3.0	6.0	Ω
$V_{CC}/2$ Generator Tolerance ($4.75\ V \le V_{CC} \le 16.5\ V$)	ϵ_r	–	–	±3.5	–	–	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)								Vdc
Low Logic State	V_{IL}	Gnd	–	V_{th} - 0.4	Gnd	–	V_{th} - 0.4	
High Logic State	V_{IH}	V_{th} + 0.4	–	18.0	V_{th} + 0.4	–	18.0	
Dynamic Total Loop Offset Voltage (Note 2)	ΣV_{offset}							mV
$I_{GC} = 12.0\ \mu A$, $V_{CC} = 12\ V$								
$T_A = 25^\circ C$		–	–	–	–	±0.5	±1.5	
$0^\circ C \le T_A \le +70^\circ C$ MC3417/18		–	–	-	–	±0.75	±2.3	
$-55^\circ C \le T_A \le +125^\circ C$ MC3517/18		–	–	-	–	±1.5	±4.0	
$I_{GC} = 33.0\ \mu A$, $V_{CC} = 12\ V$								
$T_A = 25^\circ C$		–	±2.5	±5.0	–	–	–	
$0^\circ C \le T_A \le +70^\circ C$ MC3417/18		–	±3.0	±7.5	–	–	–	
$-55^\circ C \le T_A \le +125^\circ C$ MC3517/18		–	±4.5	±10	–	–	–	
$I_{GC} = 12.0\ \mu A$, $V_{CC} = 5.0\ V$								
$T_A = 25^\circ C$		–	–	–	–	±1.0	±2.0	
$0^\circ C \le T_A \le +70^\circ C$ MC3417/18		–	–	–	–	±1.3	±2.8	
$-55^\circ C \le T_A \le +125^\circ C$ MC3517/18		–	–	–	–	±2.5	±5.0	
$I_{GC} = 33.0\ \mu A$, $V_{CC} = 5.0\ V$								
$T_A = 25^\circ C$		–	±4.0	±6.0	–	–	–	
$0^\circ C \le T_A \le +70^\circ C$ MC3417/18		–	±4.5	±8.0	–	–	–	
$-55^\circ C \le T_A \le +125^\circ C$ MC3517/18		–	±5.5	±10	–	–	–	
Digital Output Voltage								Vdc
($I_{OL} = 3.6\ mA$)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
($I_{OH} = -0.35\ mA$)	V_{OH}	V_{CC} – 1.0	V_{CC} – 0.2	–	V_{CC} – 1.0	V_{CC} – 0.2	–	
Syllabic Filter Applied Voltage (Pin 3)	$V_{I(Syl)}$	+3.2	–	V_{CC}	+3.2	–	V_{CC}	Vdc
Integrating Current	I_{Int}							
($I_{GC} = 12.0\ \mu A$)		8.0	10	12	8.0	10	12	μA
($I_{GC} = 1.5\ mA$)		1.45	1.50	1.55	1.45	1.50	1.55	mA
($I_{GC} = 3.0\ mA$)		2.75	3.0	3.25	2.75	3.0	3.25	mA
Dynamic Integrating Current Match ($I_{GC} = 1.5\ mA$)	$V_{O(Ave)}$	–	±100	±250	–	±100	±250	mV
Input Current – High Logic State ($V_{IH} = 18\ V$)	I_{IH}							μA
Digital Data Input		–	–	+5.0	–	–	+5.0	
Clock Input		–	–	+5.0	–	–	+5.0	
Encode/Decode Input		–	–	+5.0	–	–	+5.0	
Input Current – Low Logic State ($V_{IL} = 0\ V$)	I_{IL}							μA
Digital Data Input		–	–	-10	–	–	-10	
Clock Input		–	–	-360	–	–	-360	
Encode/Decode Input		–	–	-36	–	–	-36	
Clock Input, $V_{IL} = 0.4\ V$		–	–	-72	–	–	-72	

NOTE 2. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. For the MC3417/MC3517, the clock frequency is 16.0 kHz. For the MC3418/MC3518, the clock frequency is 32.0 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to insure good idle channel performance.

Table A3-2

A3-2 - Harris Devices HC-55516/HC-55532

The maximum ratings of the Harris CVSD devices are given in the following table.

Parameter	Symbol	Specified values			Units
		Min.	Typ.	Max.	
Clock bit rate	F_p		-	64	kb/s
Clock duty cycle		30	-	70	%
Supply voltage	V_{CC}	+5.0	-	+7.0	v dc
Supply current	I_{CC}	-	1.0	-	mA
Digital "1" input	V_{IH}	-	4.5	-	v
Digital "0" input	V_{IL}	-	1.5	-	v
Digital "1" output	V_{OH}	-	5.5	-	v
Digital "0" output	V_{OL}	-	0.5	-	v
Audio input voltage	V_I	-	0.5	1.4	v_{rms}
Audio output voltage	V_O	-	0.5	1.4	v_{rms}
Audio input impedance	Z_{in}	-	100	-	KΩ
Audio output impedance	Z_{out}	-	100	-	KΩ
Transfer gain	A	-0.5	-	+0.5	DB
Syllabic filter time constant	T_S	-	4.0	-	ms
L.P. Filter time constant (55516)	T_{LP}	-	0.94	-	ms
(55532)		-	0.47	-	ms
Step-size ratio (55516)		-	24	-	DB
(55532)		-	18	-	DB
Resolution (55516)		-	0.1	-	% of V_{CC}
(55532)		-	0.2	-	% of V_{CC}
Min step-size (55516)		-	0.2	-	% of V_{CC}
(55532)		-	0.4	-	% of V_{CC}

Parameter	Symbol	Specified value			Units
		Min.	Typ.	Max.	
Quieting pattern (55516) amplitude	Δ_{min}	-	12	-	mv_{p-p}
(55532)		-	24	-	mv_{p-p}

Test conditions V_{CC} = 6.0

F_P = 16.0 kb/s (HC-55516)

= 32.0 kb/s (HC-55532)

T_A = 25°C

Table A3-3 - Absolute maximum ratings and electrical characteristics of the Harris device.

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